Digital Systems Problem Set #1

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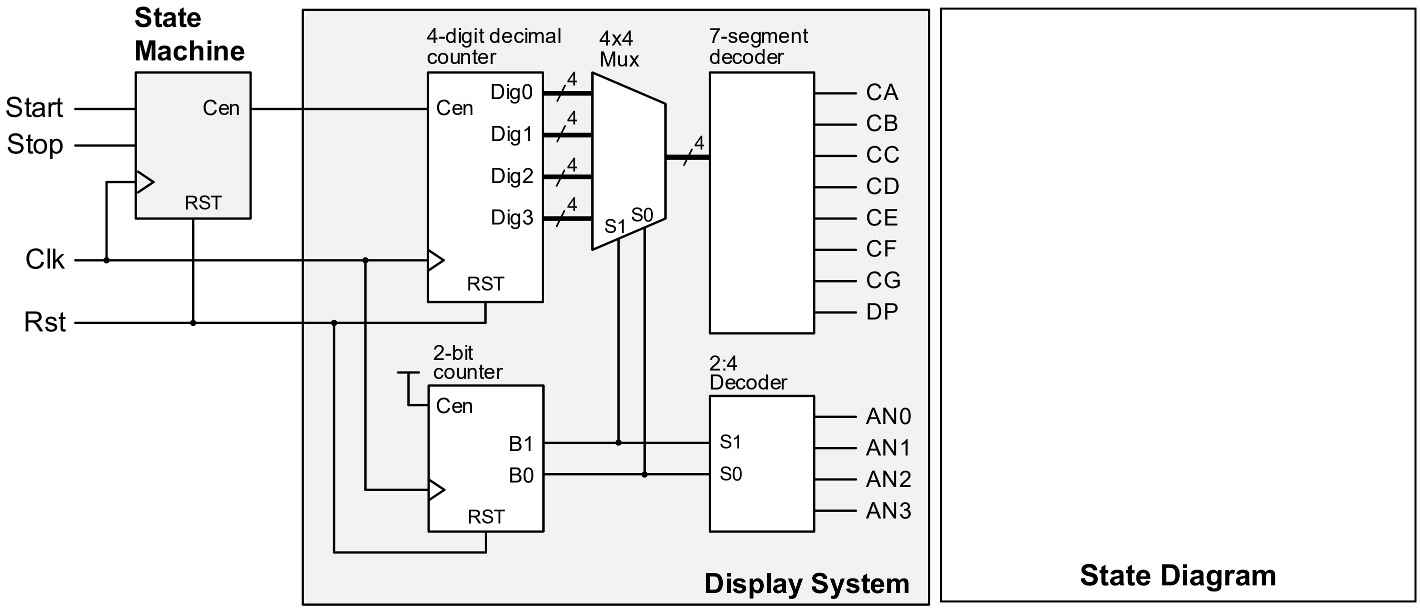
1. (10 points) Design a simple state machine to control a timer circuit that can drive the circuit as shown below. The timer output is always displayed on the 7-segment display. Your state machine receives two inputs, START and STOP. When START is pressed, the timer should count up; when STOP is pressed, the counter should stop counting and the display should show the current timer output. Sketch a state diagram for the controller, and then write Verilog code to describe its behavior.



```
module P1 (


);





always @ (posedge(clk),posedge(rst))








endmodule
```

2. (20 points) Enter T or ***leave blank for False*** for each statement below.

□ A state machine that uses a state register with 3 flip-flops can be in any one of 16 states

□ A seven-segment decoder implements four logic functions of seven variables each

□ A NOR gate uses fewer transistors than a NAND gate

□ In Verilog, it is permissible to assign a wire from inside an always block

□ The output of a transparent D-latch can only change on the rising edge of the clock signal

□ An RCA is smaller and faster than a CLA

□ When instantiating a component, your code must refer to the *source file* name that contains that component

□ It is possible to write a Verilog always block that defines purely combinational logic

□ When writing structural Verilog, the keyword "Structural" must appear in your first line of code

□ Right-shifting a binary number by two bits is the same as multiplying by 4

□ In the Xilinx tool set, you must synthesize Verilog code before it can be simulated

□ Flip-flops are inferred in Verilog using the key word "flipflop" in the first line of a module statement

□ The main input clock on the Blackboard comes from a 1MHz oscillator

□ To simulate a Verilog file, you must write another Verilog source file called a "test harness activator"

□ Any Verilog module can be used as a component in any other Verilog module

□ When you program the Blackboard, your Verilog code is executed on the ZYNQ ARM processor

□ Every possible logic function has a minimal SOP form, but only some have a minimal POS form

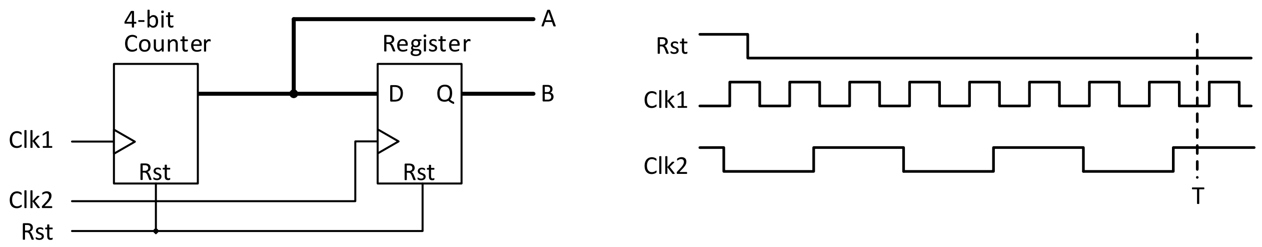
□ A truth table with 6 input variables would have 72 rows

□ You must be sure to write Verilog "assign" statements in the proper order for accurate simulations

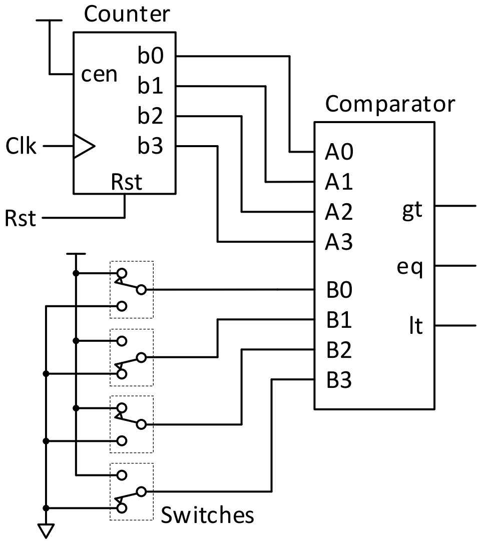
□ In the Viviado tool, physical pin numbers are assigned to signals in the "pin-mappings.bs" file

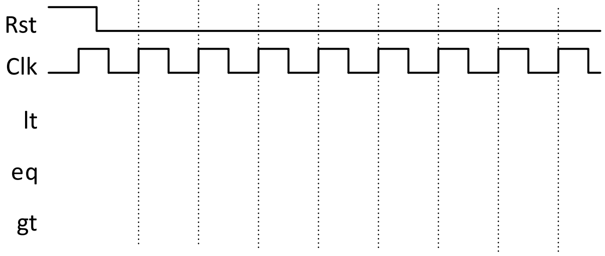
3. (4 points) In the figure below, what are the values at time T for the counter output (A) and the register output (B)?

A _____ B_____

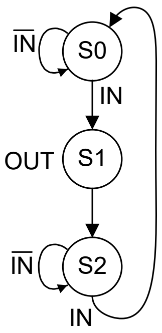


4. (6 points) Complete the timing diagram to show how the signals gt, eq, and lt change over time

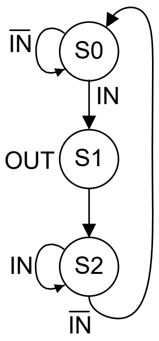




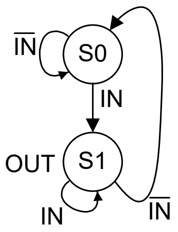
5. (4 points) One of the state diagrams defines a circuit that can assert an output (OUT) for one clock period each time an input (IN) is asserted, regardless of how long IN is asserted. Circle the letter of the appropriate diagram.



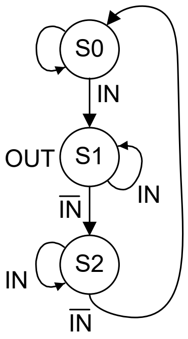
A



B



C

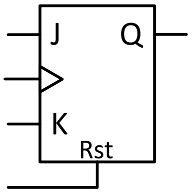


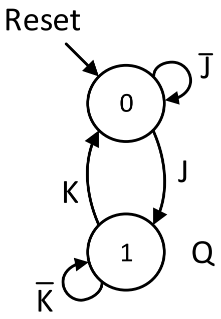
D

6. (6 pts) Write a Verilog statement that defines a *minimum* circuit for: Y <= Σm(2, 4, 5, 6, 10, 12, 13, 14).

7. (10 points) Write Verilog code for a JK flip-flop

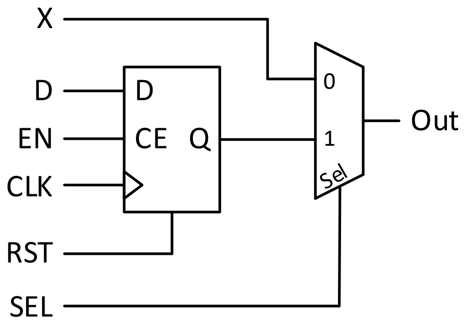
```
module HW1  (input
             output                        );
```





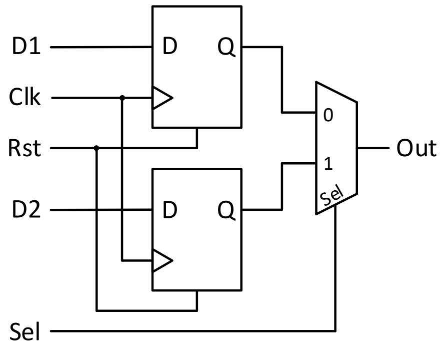
8. (10 points) Complete Verilog code to describe the circuit shown.

```
module HW2 (input X, D, EN, CLK, RST, SEL
            output Out);
```

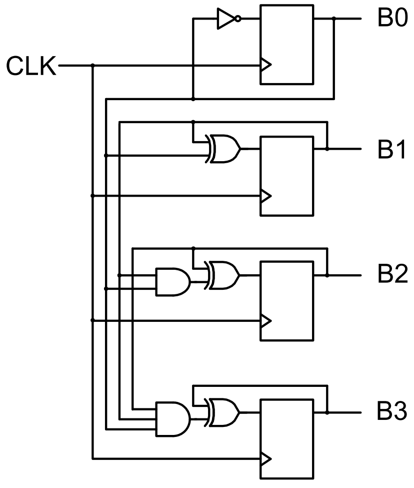


9. (10 points) Complete Verilog code to describe the circuit shown.

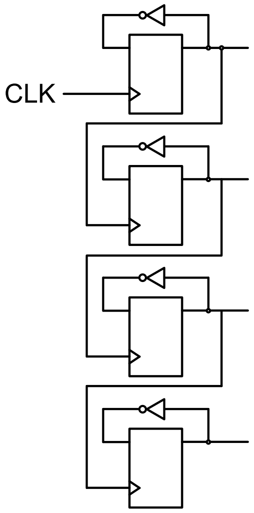
```
module HW3 (input clk, rst, D1, D2, Sel
            output Out);
```



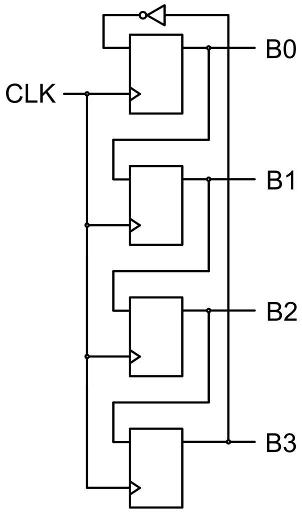
10. (12 points) The figures below show three different types of 4-bit counters. Enter a '1' in the columns labeled A, B, and C if the feature applies, and a '0' if it does not.



A



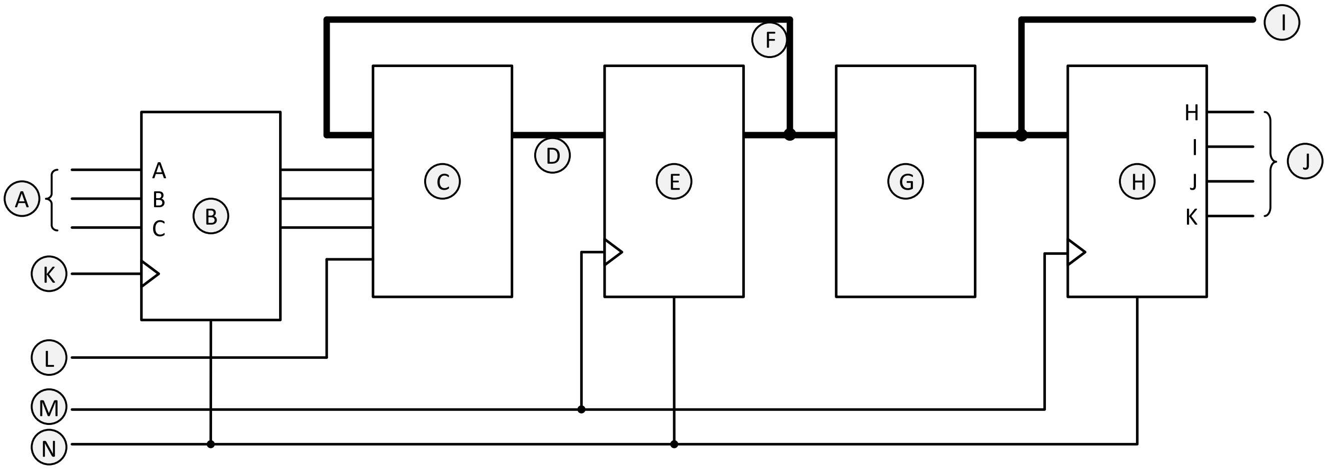
B



C

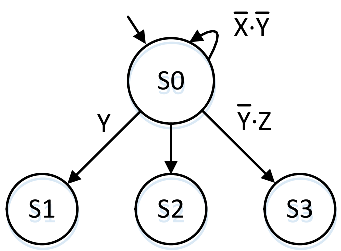
#	A	B	C	Feature
1				Creates 2^N binary numbers from N flip-flops
2				Suffers from output-bit skew problems in higher-order bits
3				Is not limited in operating frequency by next-state logic delays
4				Is commonly called an Asynchronous Counter
5				Is commonly called a Ring or Johnson Counter
6				Is commonly called a Binary Counter
7				Creates (2 x N) binary numbers from N flip-flops
8				Outputs (bit signals B0 – B3) can have glitches
9				Outputs (bit signals B0 – B3) can be used as clocks for other circuit blocks
10				Generates numbers in a natural counting sequence (0,1, 2, 3, etc)
11				Can be used as a memory register in a state machine
12				Can be limited in operating frequency by next-state logic delays

11. (16 points) A block diagram for a circuit that contains a state machine is shown below. Associate the lettered items with the best description, and enter the letters in the table below. Some letters may be used more than once, and some descriptions may not have an associated letter.



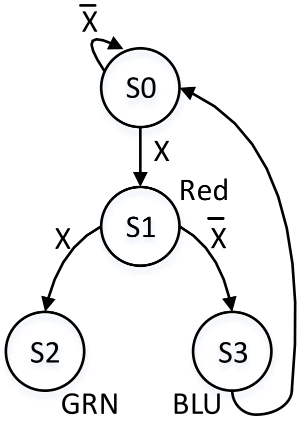
		These two blocks contain only combinational logic
		Delay in this block is the primary determinant of overall clock speed for this circuit
		This block may need its own state machine
		These outputs are gitch-free
		The number of flip-flops here determine how many states are possible
		Best place for a de-metastabilizing and/or debouncing circuit
		This circuit can eliminate/filter potential output race glitches and other logic noise
		The binary number stored here defines the state of the state machine
		This block could contain a Ring or Binary counter
		Delay here may skew the combinational output signals, but won’t limit how fast the state machine can run
		Glitches and hazards in this circuit can generate “logic noise” on outputs
		This input is not synchronized locally, and so the “go/no-go” configuration should be used
		These outputs may have glitches
		Using a block like this means you don’t need to use the GO/NO-GO method for dealing with inputs
		The maximum frequency this signal can be driven at is determined by the delay in block C

12. (4 points) No branch condition is shown for the S2 branch. If some combination of branch conditions exists for which no next state is specified, then make that combination the S2 branch condition. Then, modify the hold condition so that only one next state is specified for all combinations of branch conditions. Enter the branch conditions below.

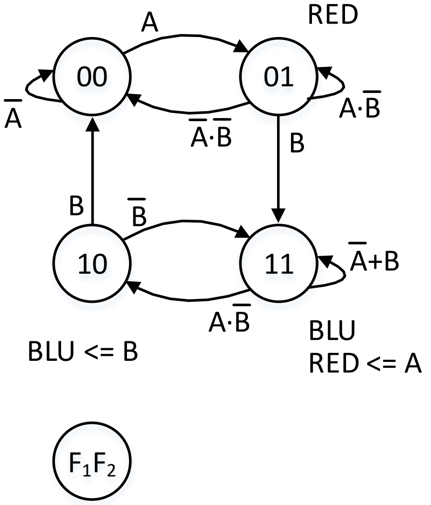


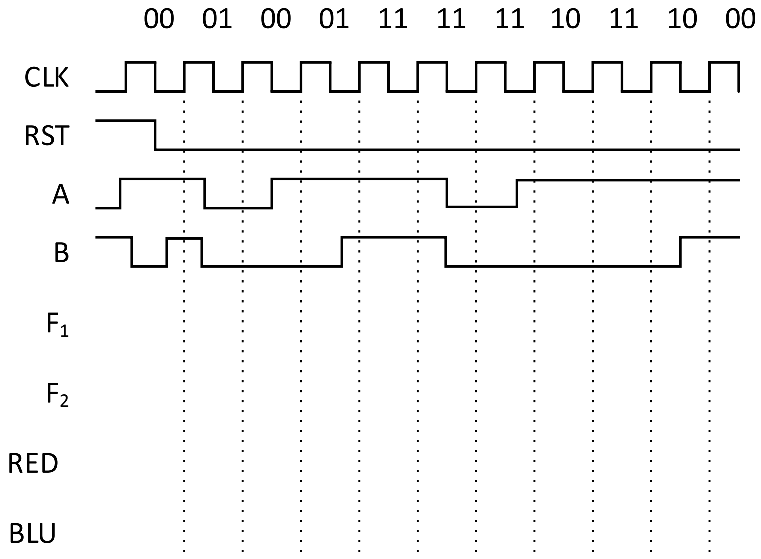
To S2:____________ Holding condition:____________

13. (8 points) A state machine receives an input X that is synchronous with the system clock. If X is a 1, then the machine must output a signal RED for one clock cycle. Then, if X is still asserted, the machine must output a signal GRN for one clock cycle, but if X is not asserted, the machine must assert an output called BLU. The state diagram below meets these requirements. Sketch a diagram that can meet these same requirements, but that uses just one flip-flop.

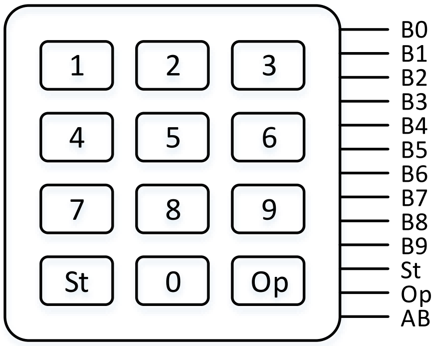


14. (12 points) In the timing diagram below, show the time courses of the flip-flops (labeled A and B) and output signals defined by the state diagram.





15. (15 points) Sketch a Moore-model and also a Mealy-model state diagram for a sequential machine that can detect when a four-digit combination has been typed into a numeric keypad. Use last four numbers of your telephone number for a combination. A “start” button must be pressed immediately prior to entering a valid combination, and an “open” button must be pressed immediately after a valid combination. For this problem, you can assume that two buttons cannot be asserted simultaneously (i.e., if more than one button is pressed, only the signal from the first button pressed will be asserted until it is released; the second button will be asserted after the first button is released if it is still being pressed. If more than two buttons are pressed, and the first button pressed is released, then the second button pressed will be asserted until it is released, and so forth). The “Any Button” (AB) output will be asserted as soon as any button is pressed, and de-asserted only when no buttons are pressed.


1
2
3
4
5
6
7
8
9
St
0
Op
B0
B1
B2
B3
B4
B5
B6
B7
B8
B9
St
Op
AB