

AUP-ZU3

Variant: Prototype

1/30/2025

V3I1

RELEASED

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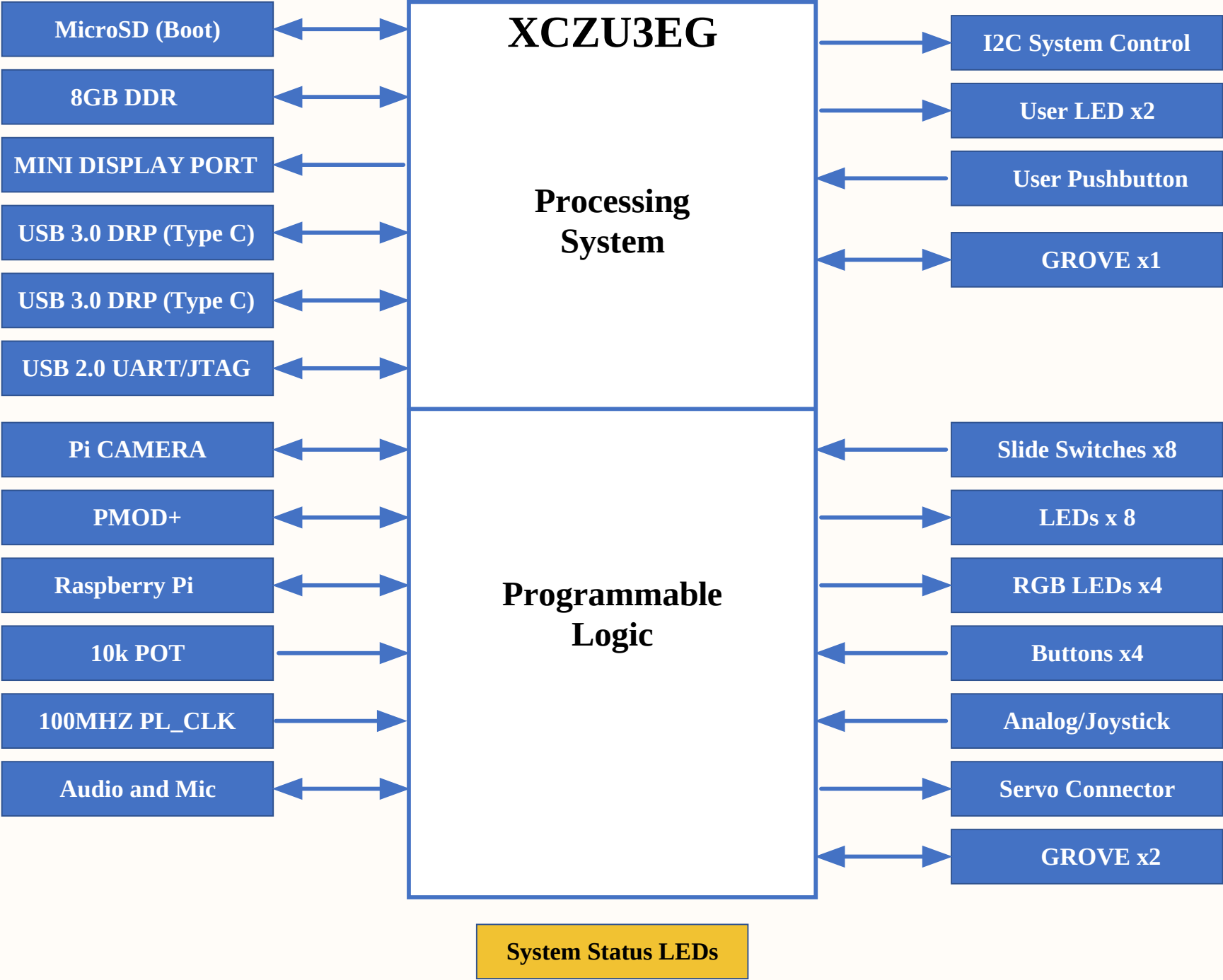
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AUP-ZU3

(Block Diagram)



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AUP-ZU3

(Power Diagram)

UNITS

CONNECTION

Legend

IC

Programmable Logic

Connector

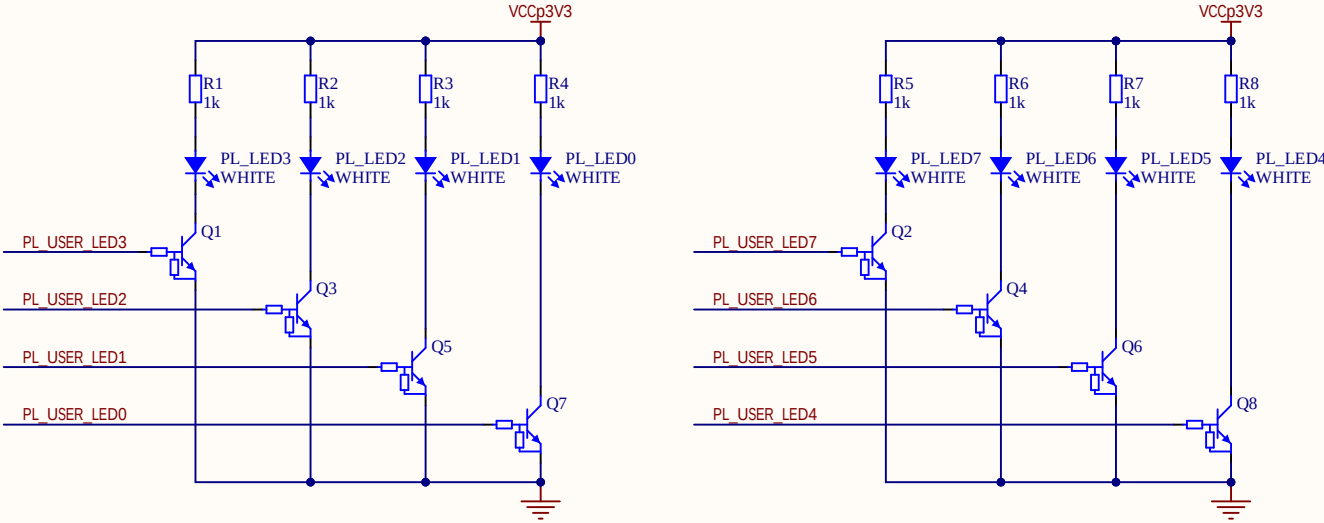
Processor System

MISC

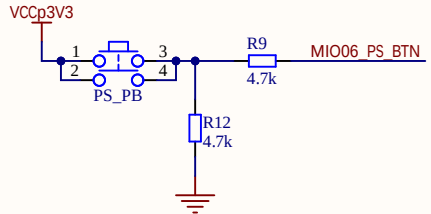
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USER IO, LEDs

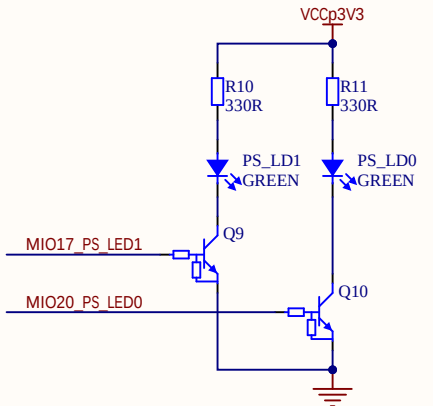
PL user-defined white LEDs



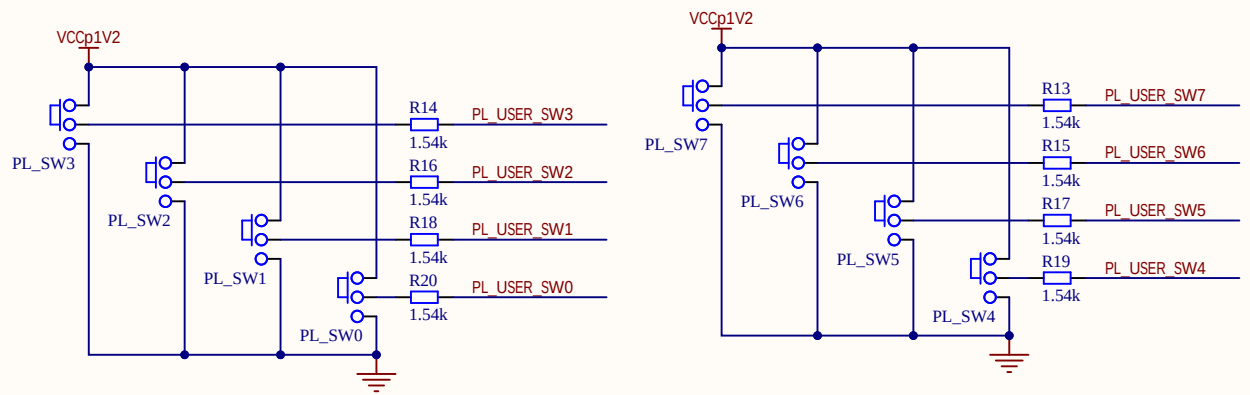
PS user-defined pushbutton



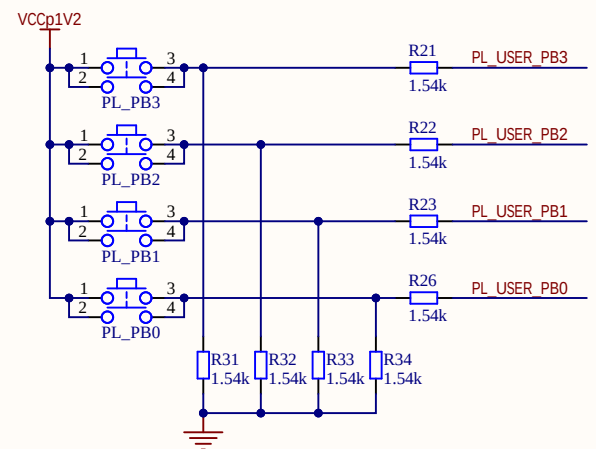
PS user-defined green LEDs



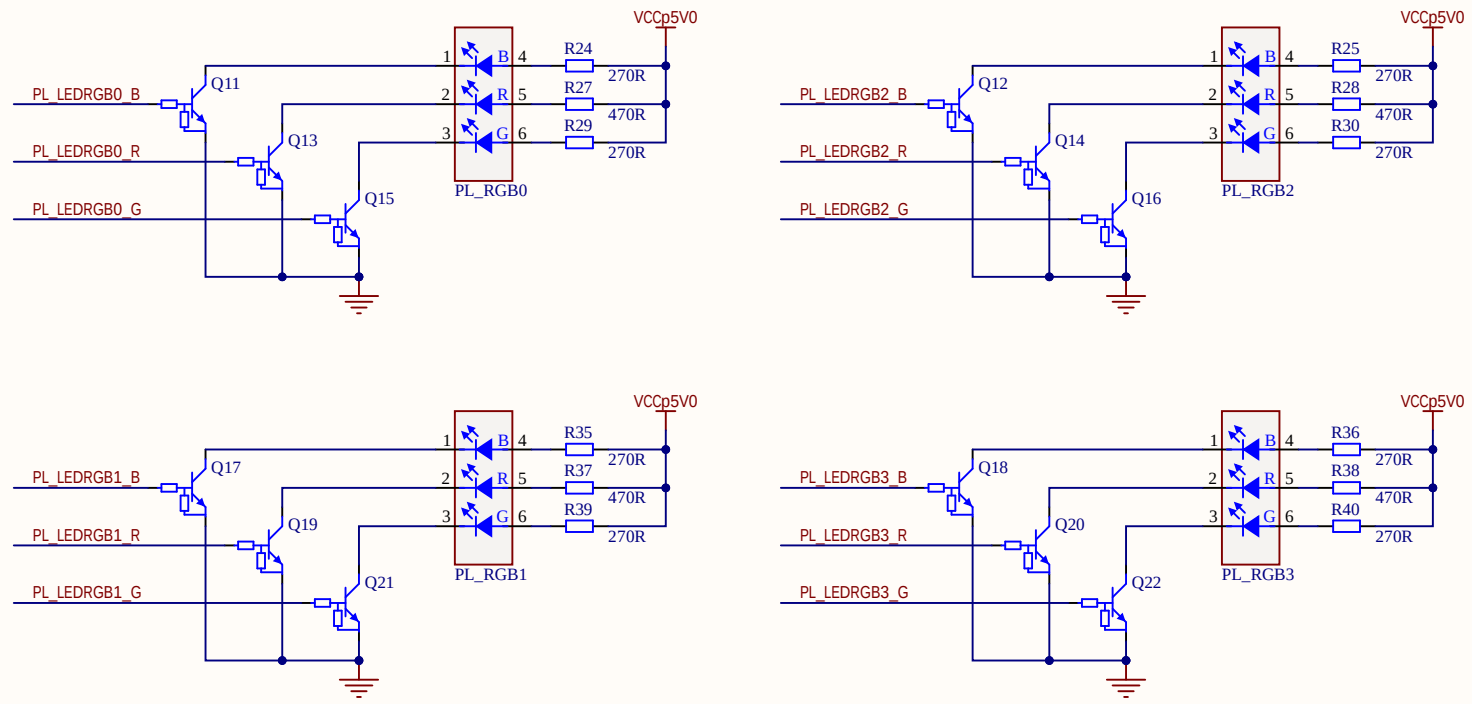
PL user-defined switches



PL user-defined pushbuttons



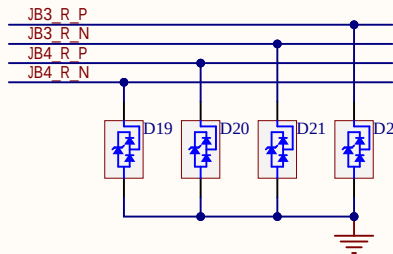
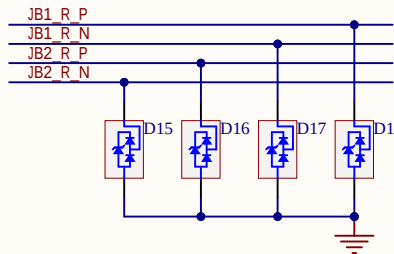
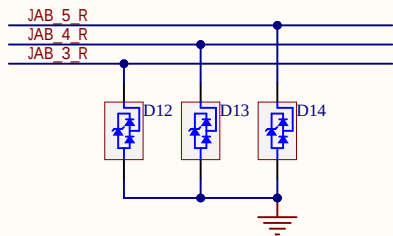
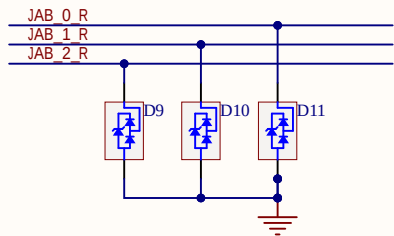
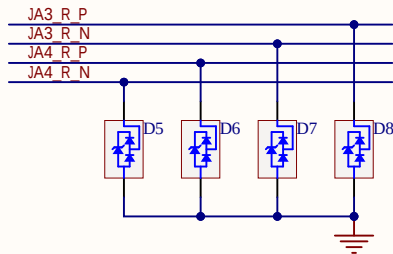
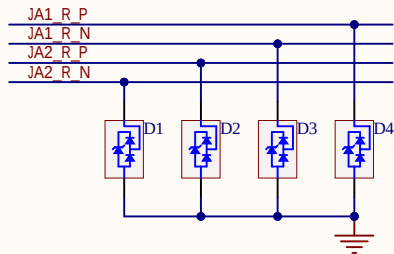
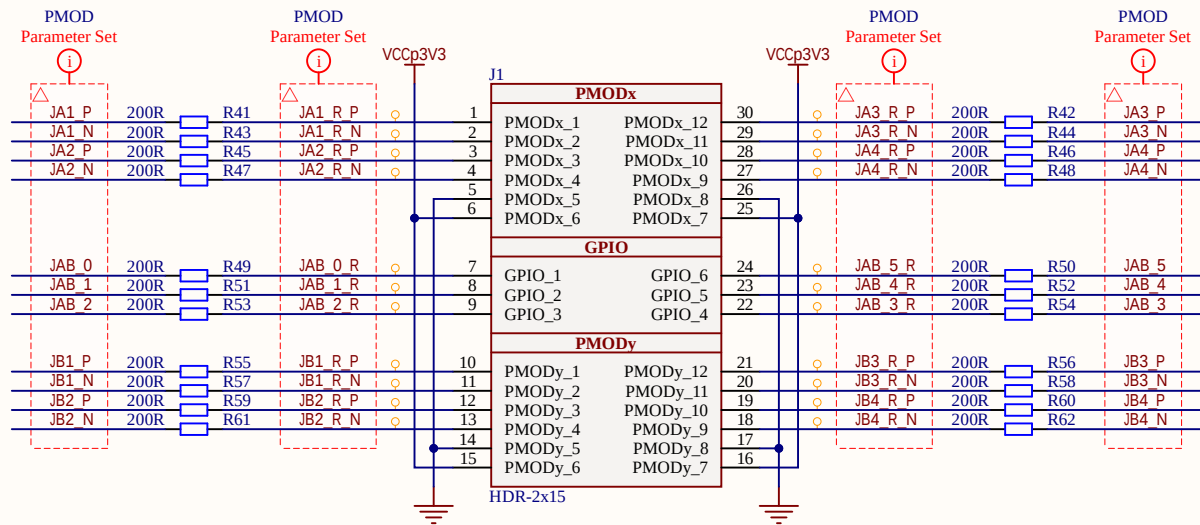
PL user-defined RGB LEDs



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PMOD HEADERS

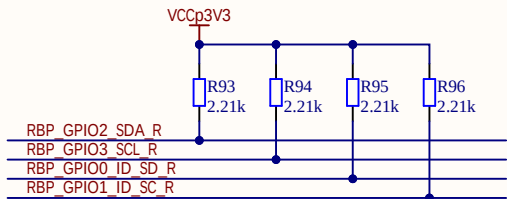
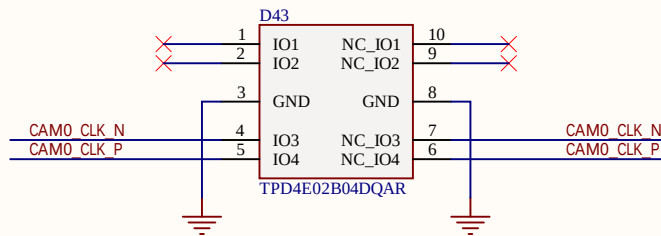
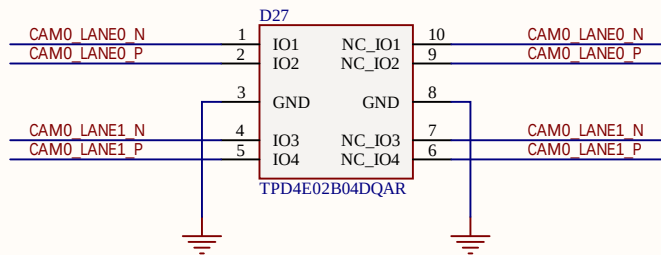
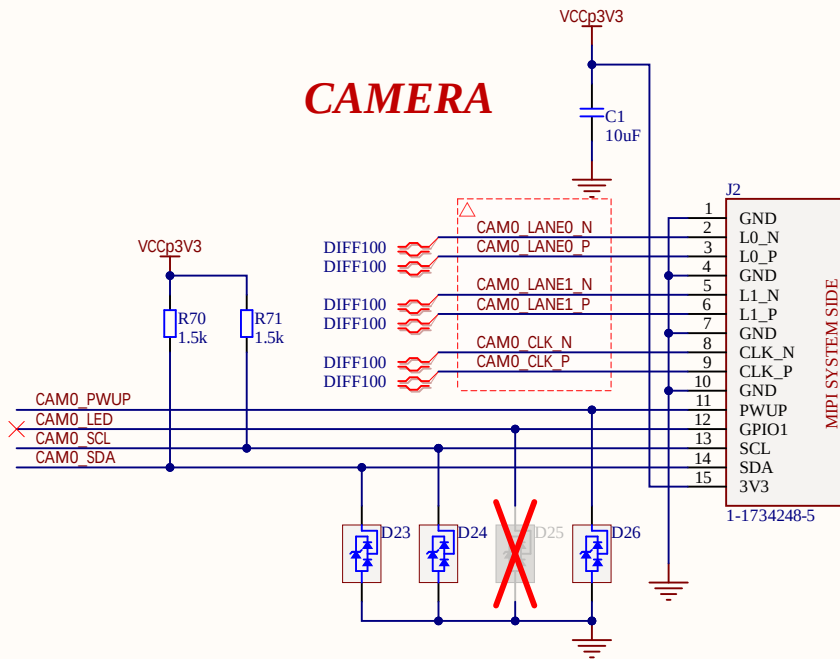
PMOD A and B



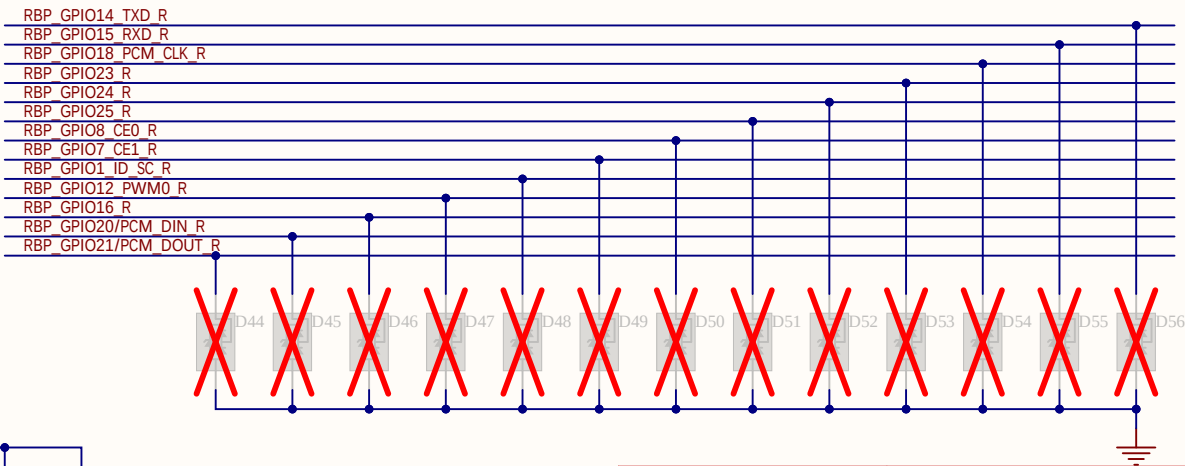
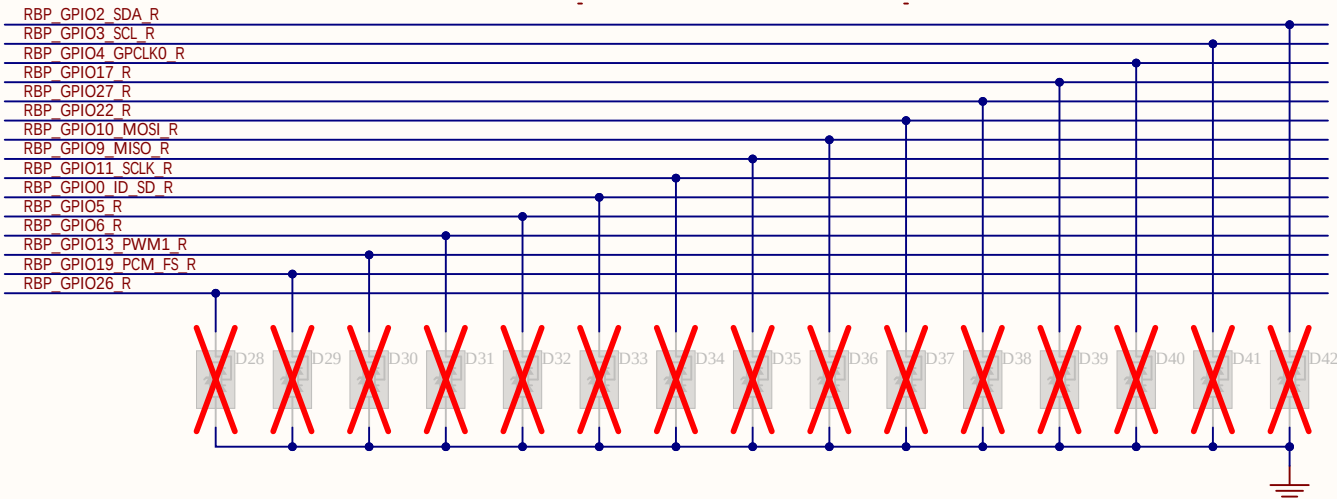
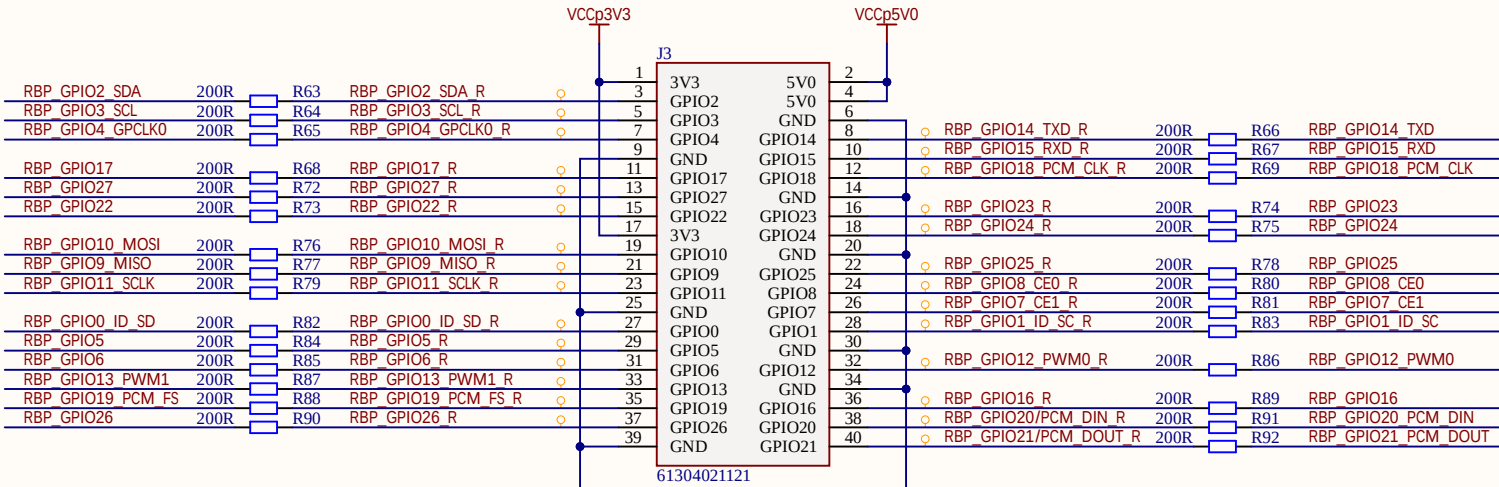


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CAMERA AND RPI

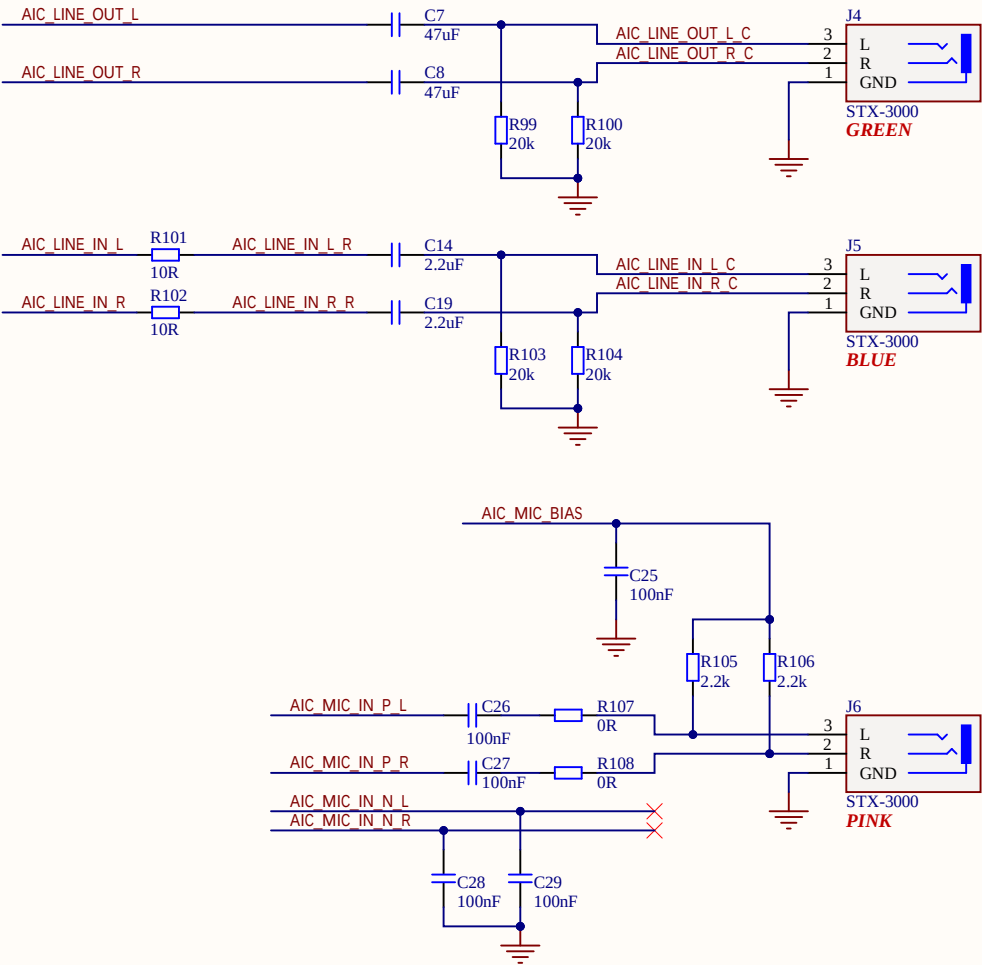
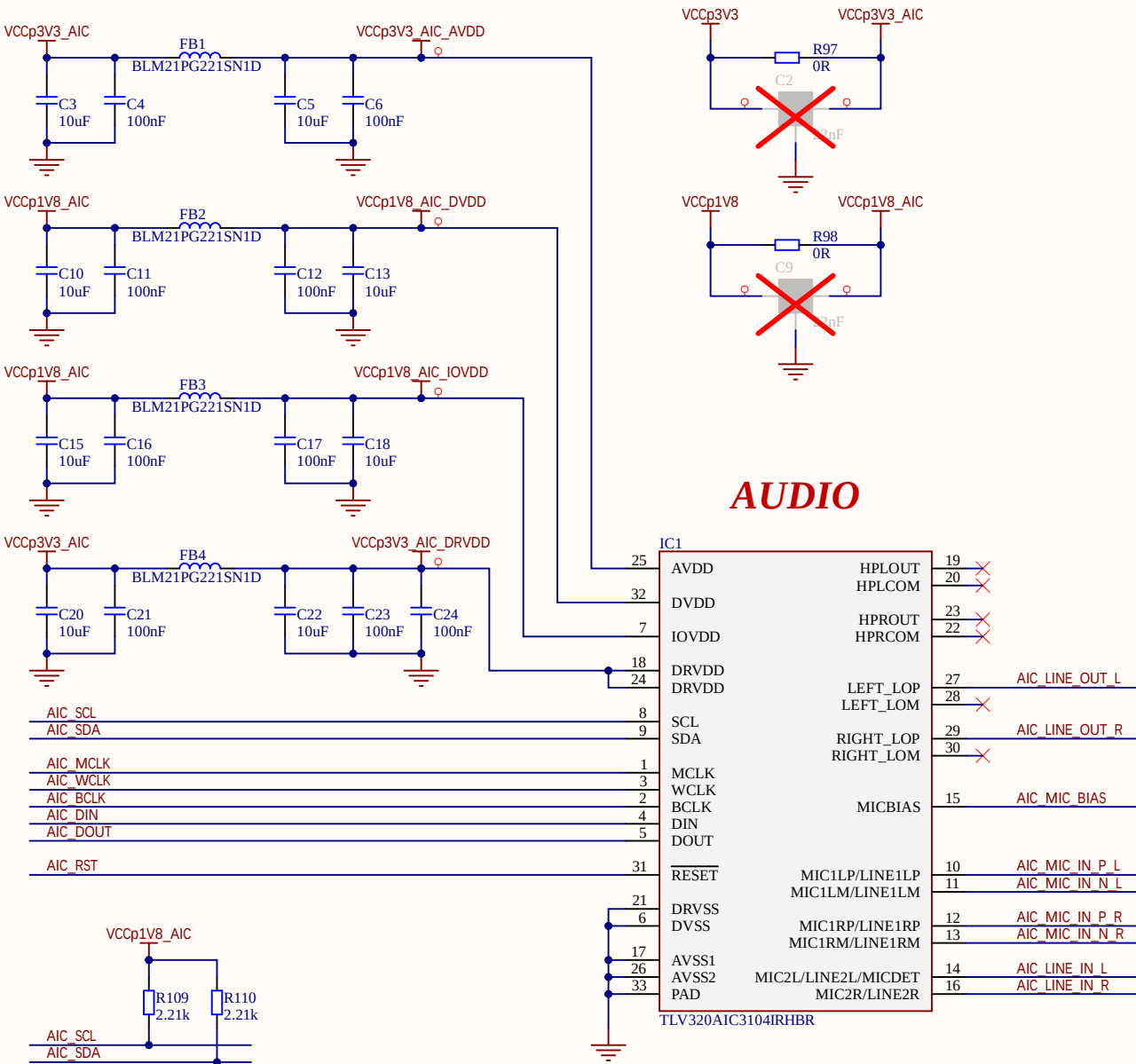


RASPBERRY Pi HAT EXTENSION



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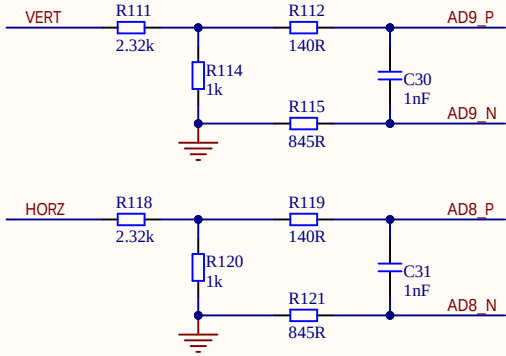
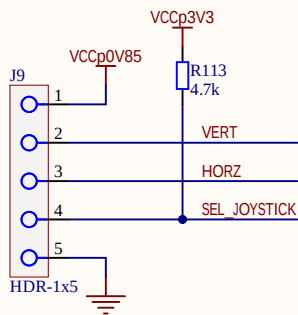
AUDIO AND MIC



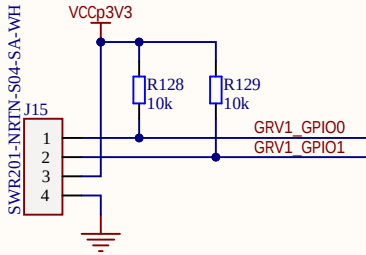
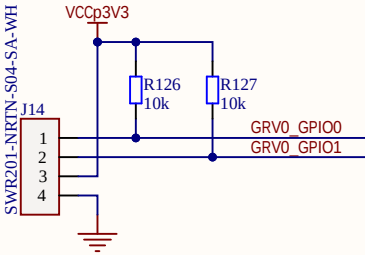
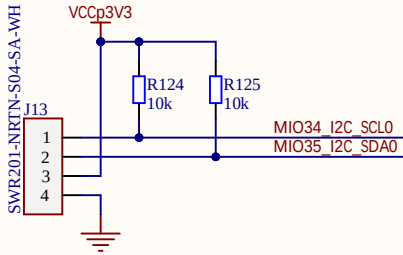
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ANALOG AND SERVO

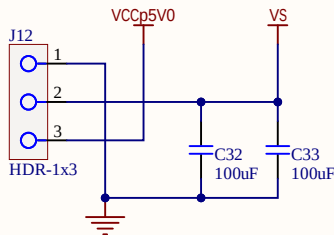
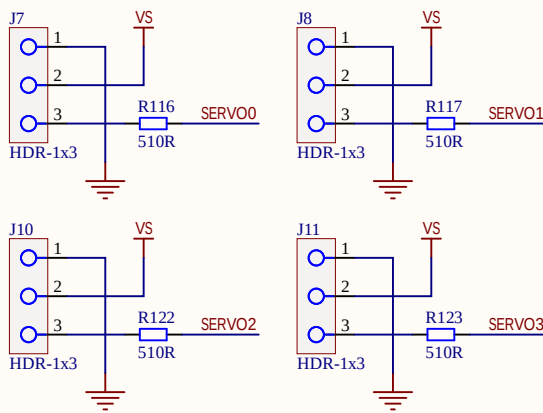
JOYSTICK



GROVE

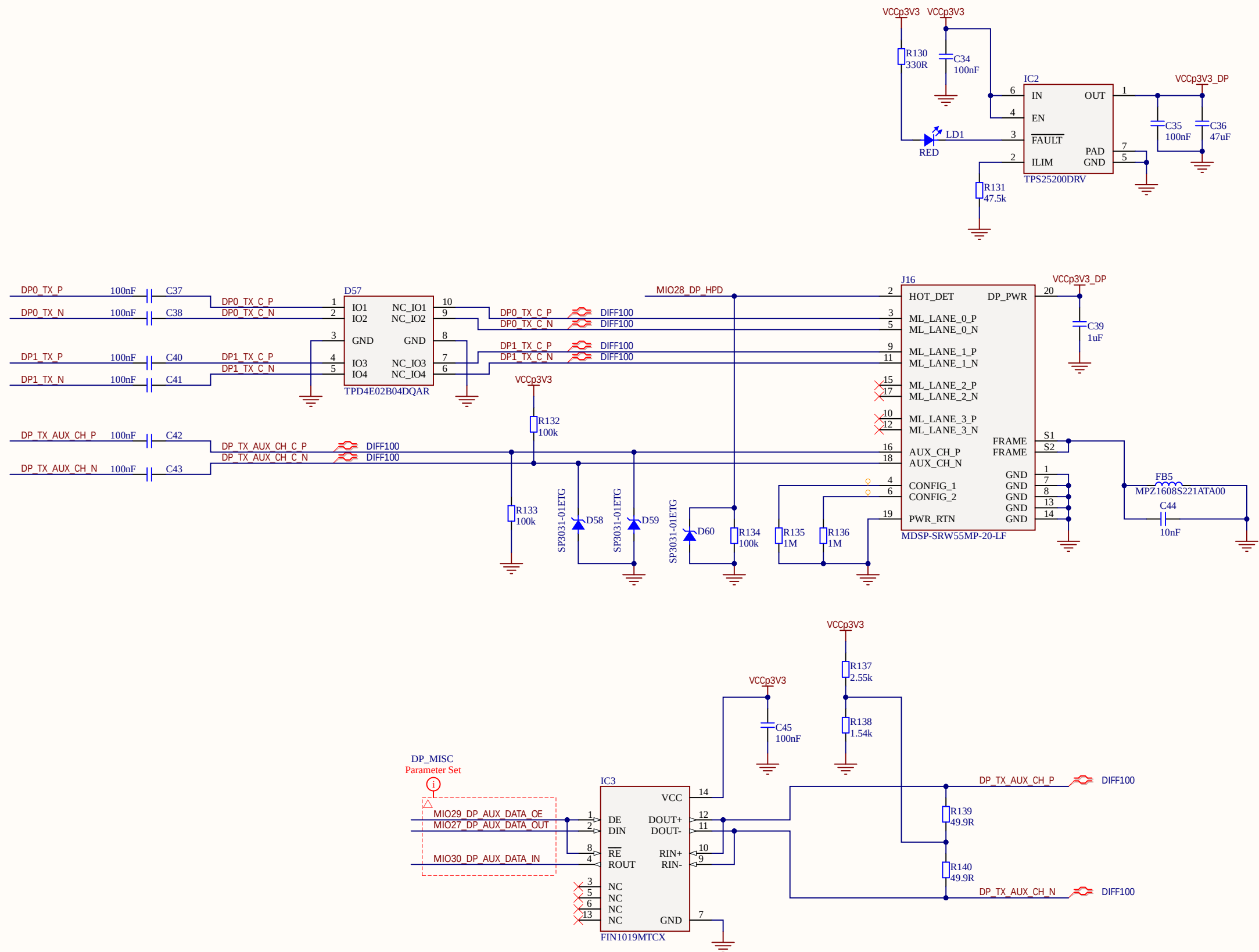


SERVO



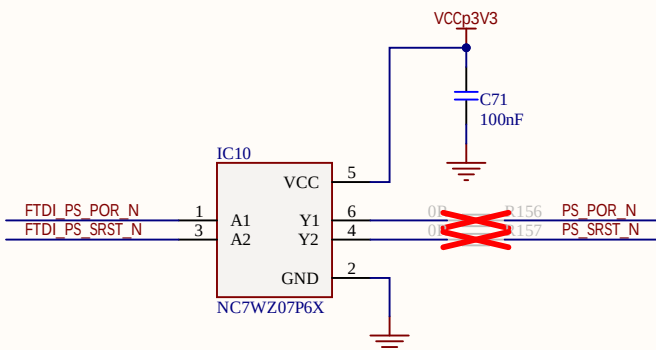
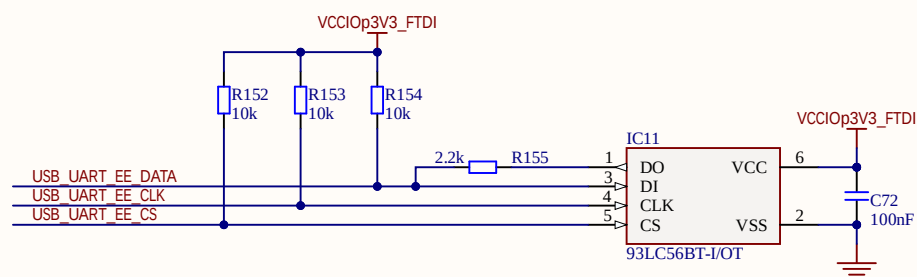
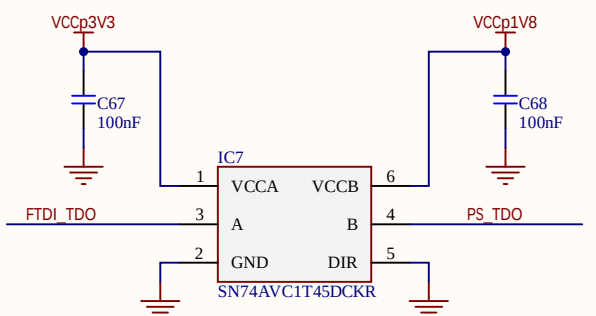
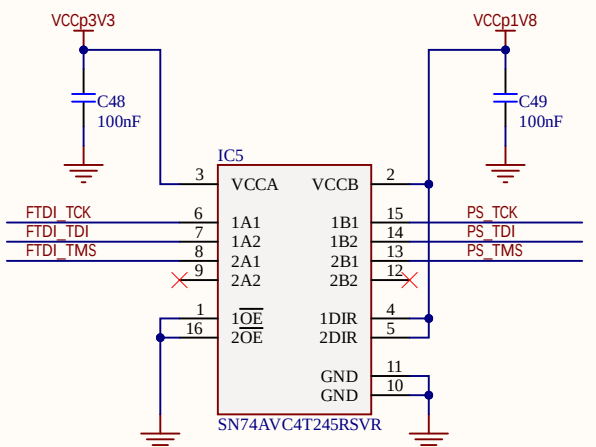
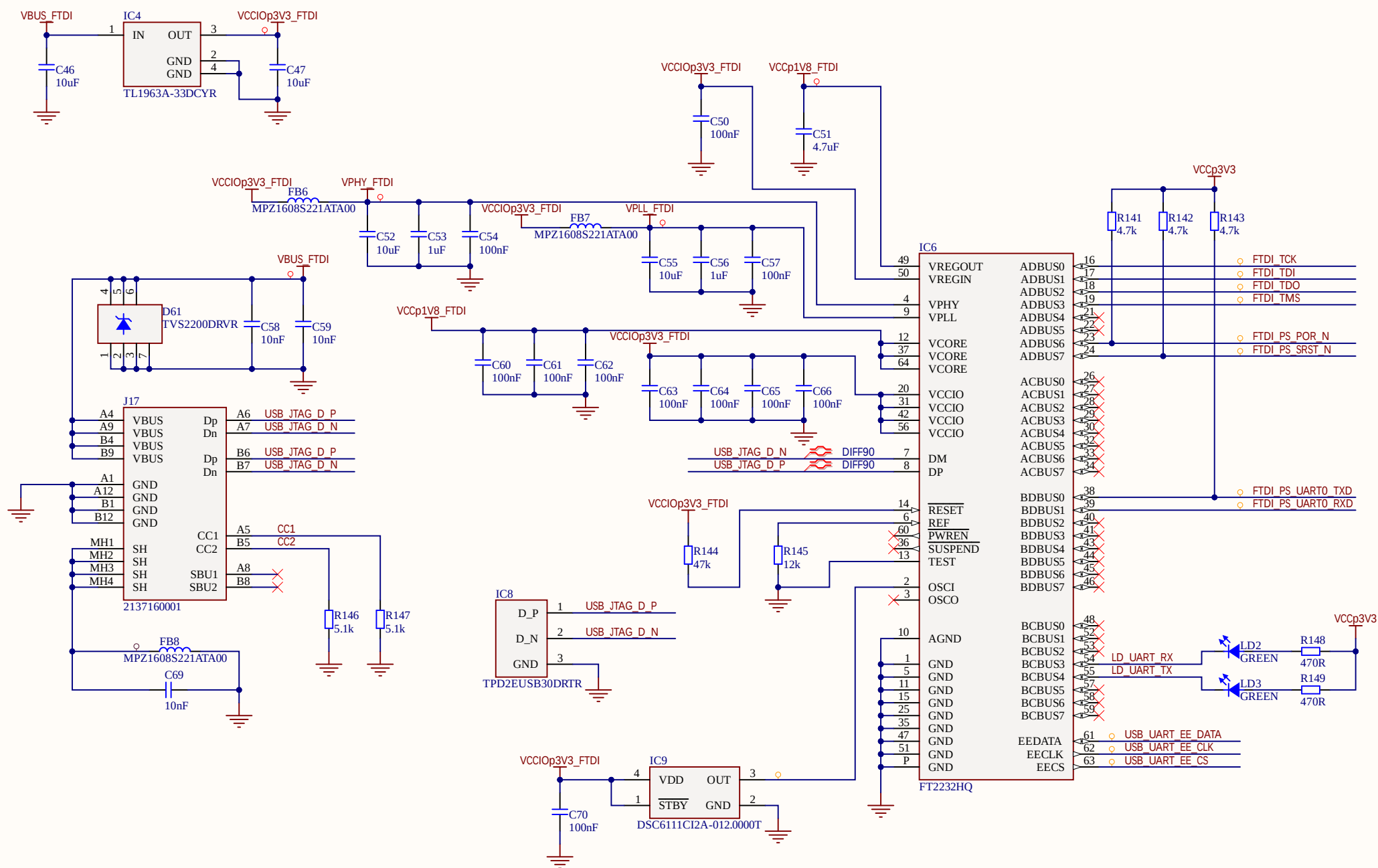
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DISPLAY PORT



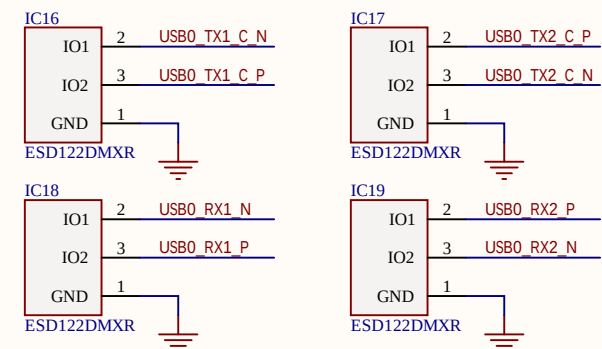
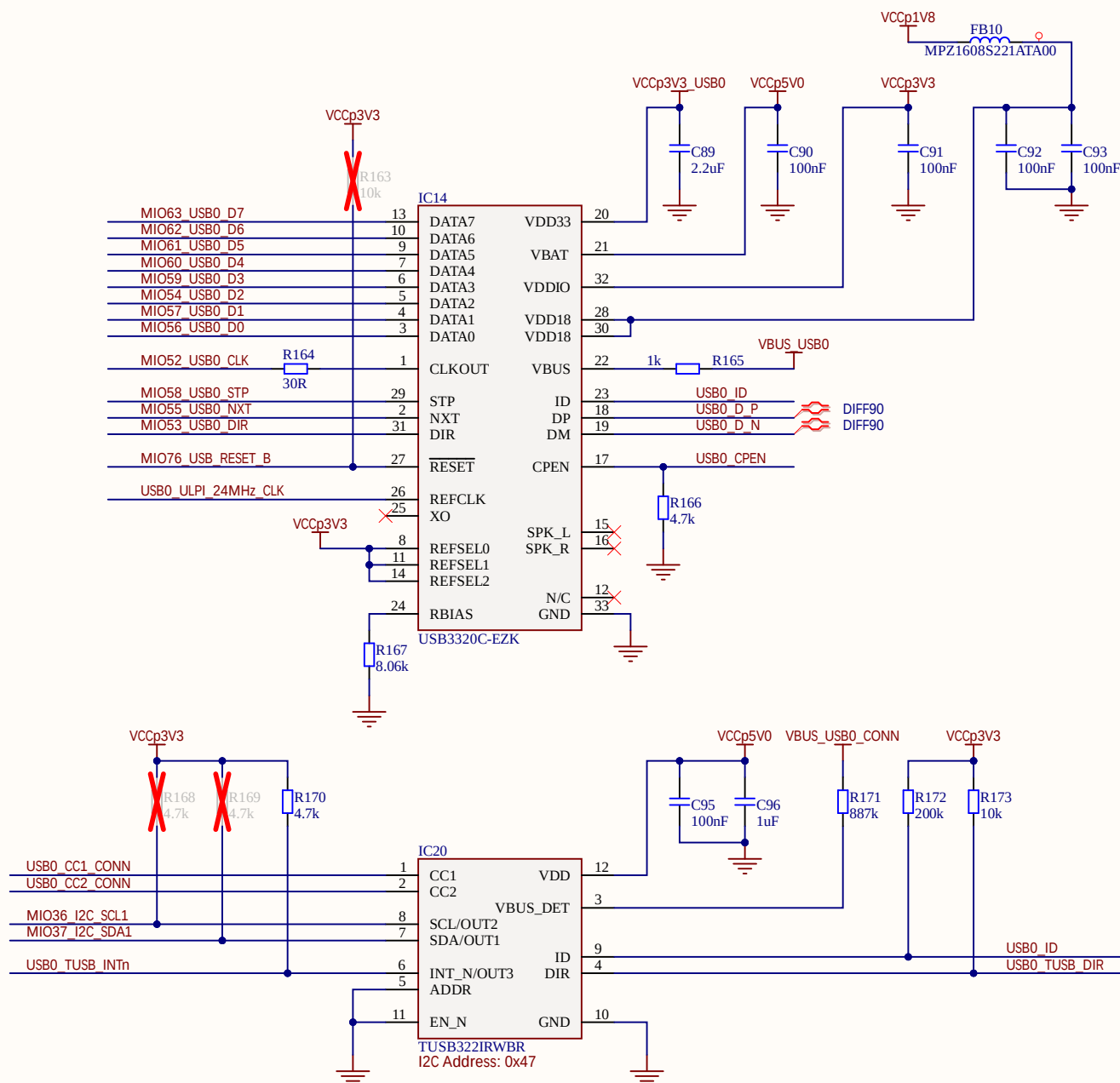
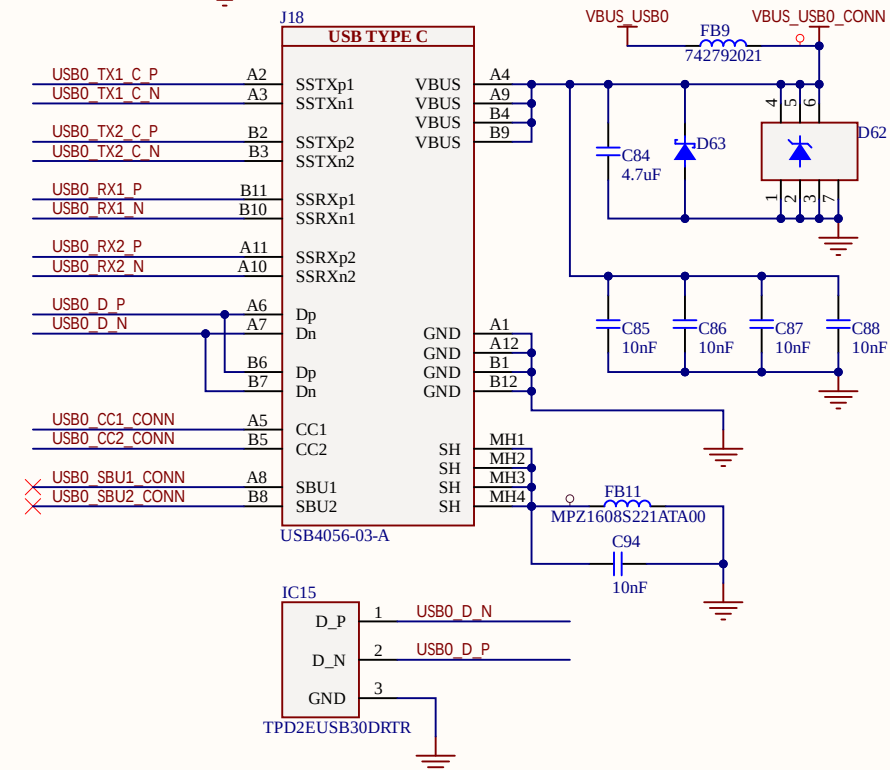
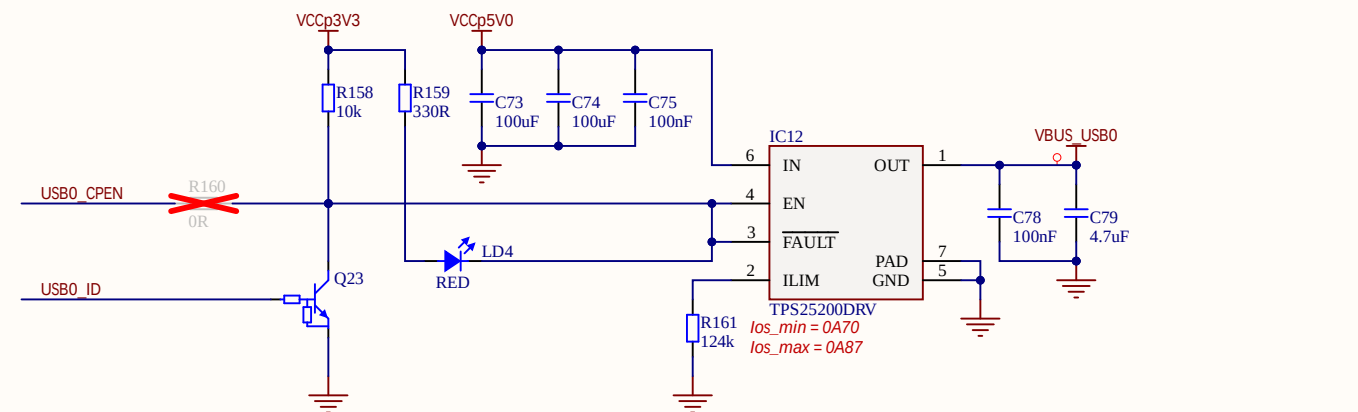
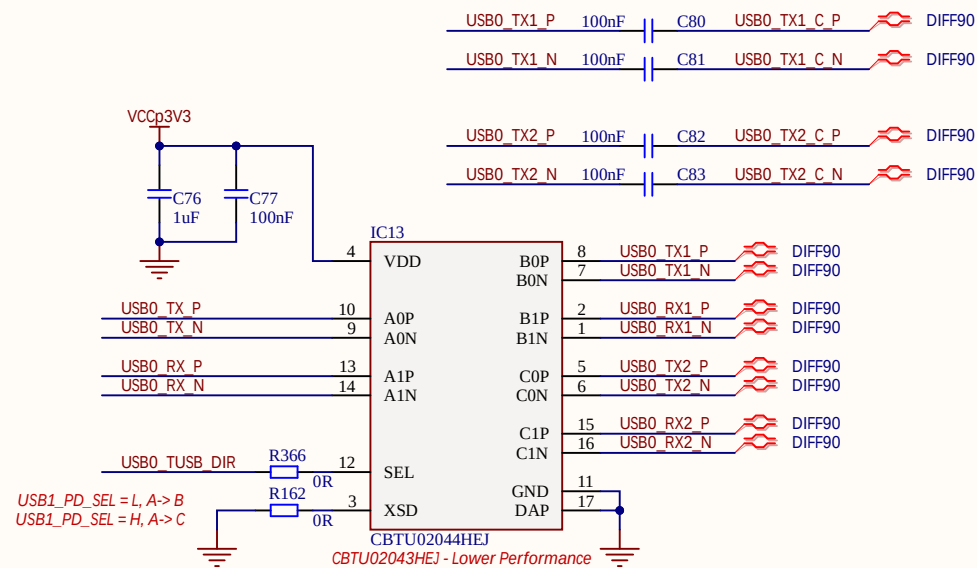
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USB-JTAG, USB-UART



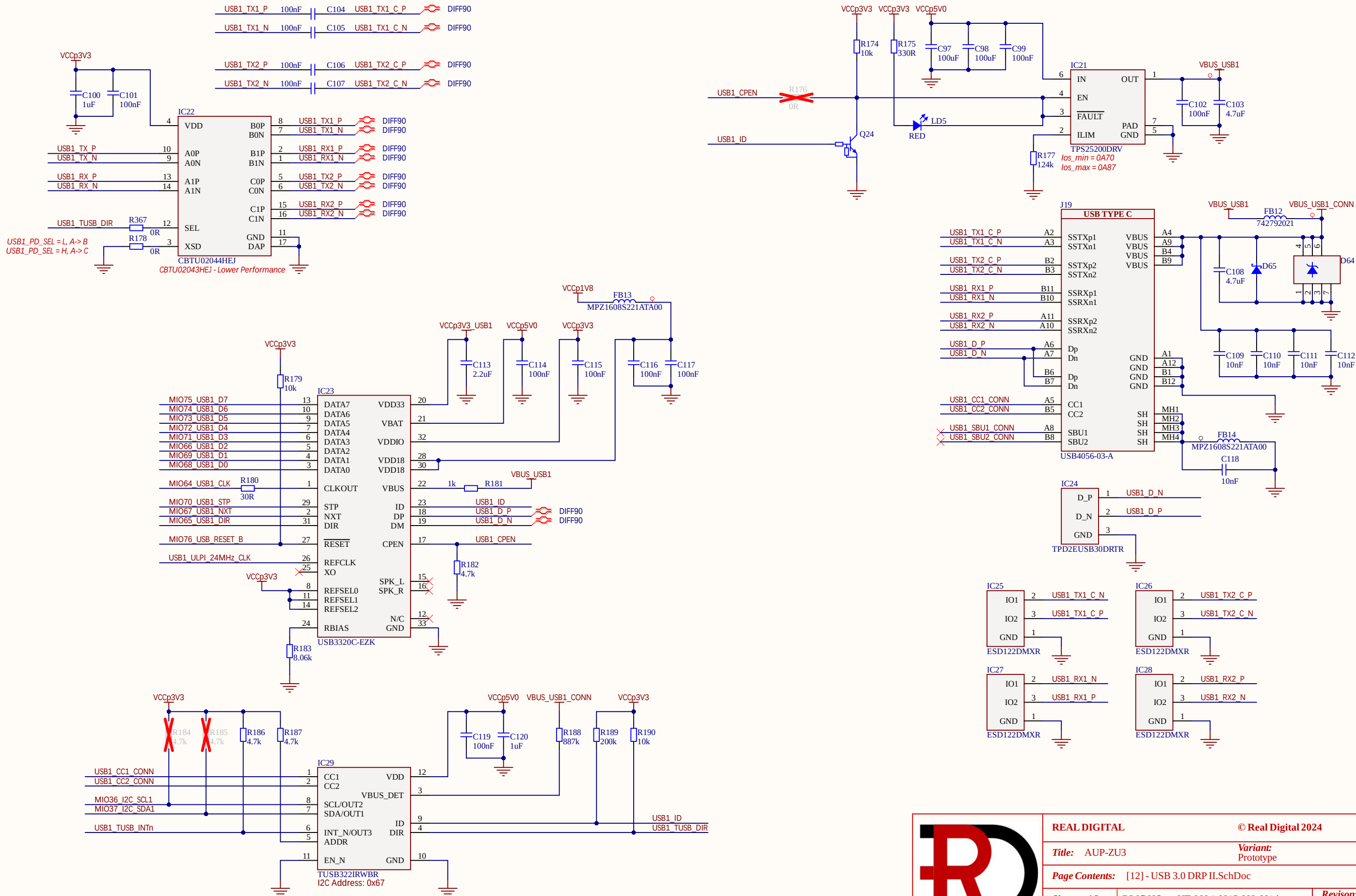
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USB 3.0 DRP I



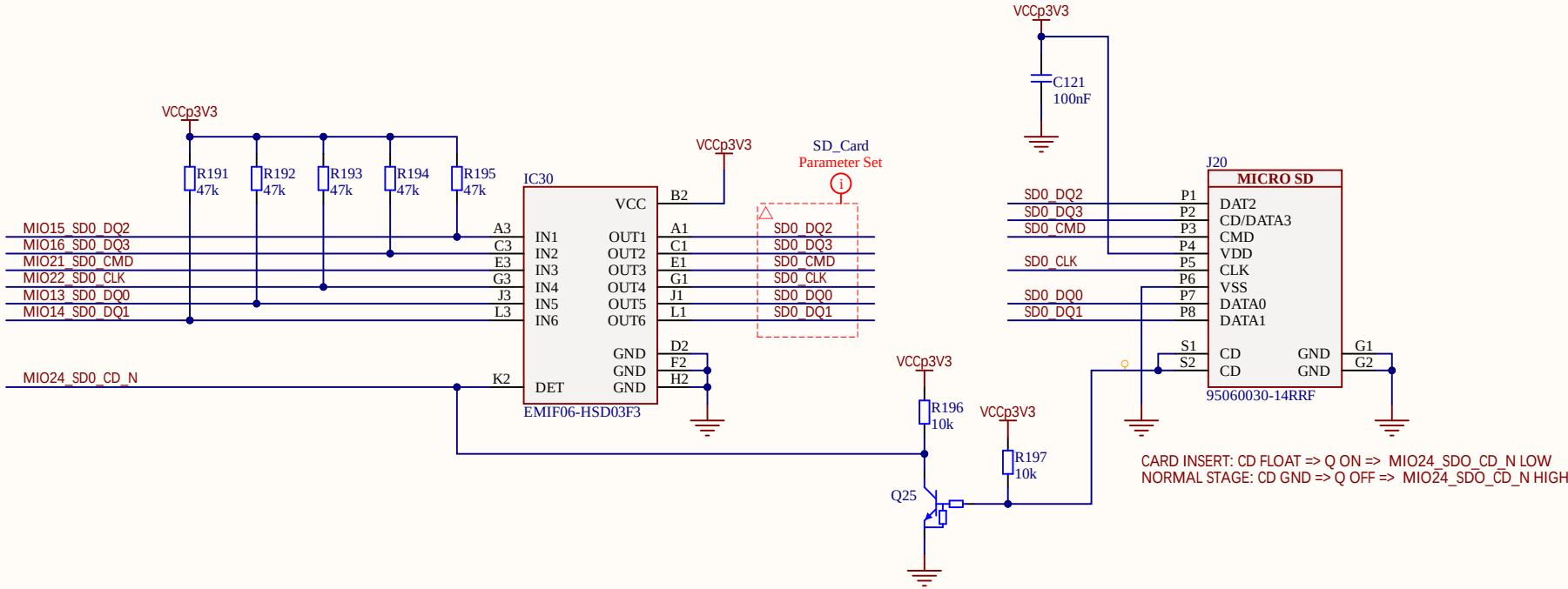
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USB 3.0 DRP II



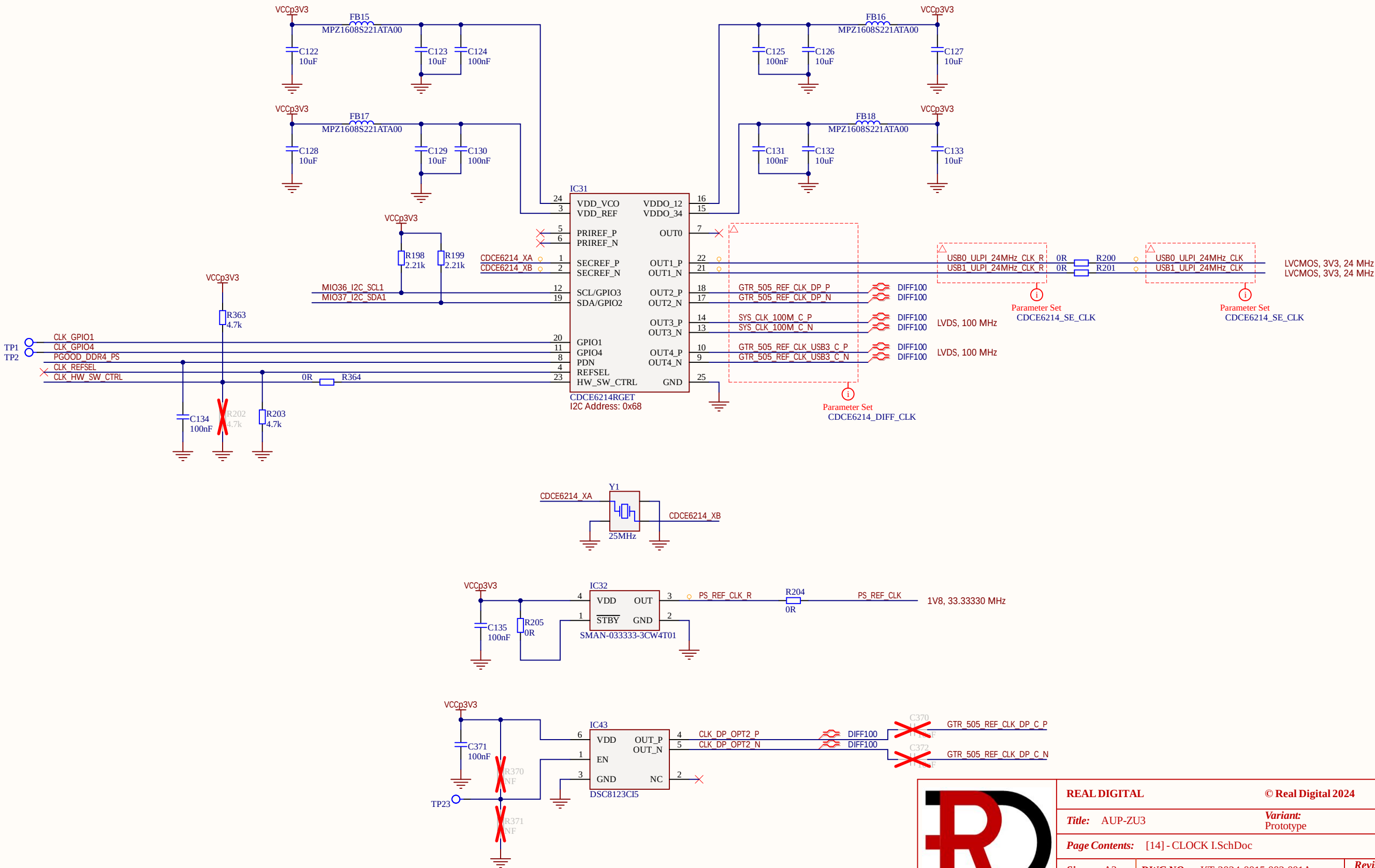
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SD CARD



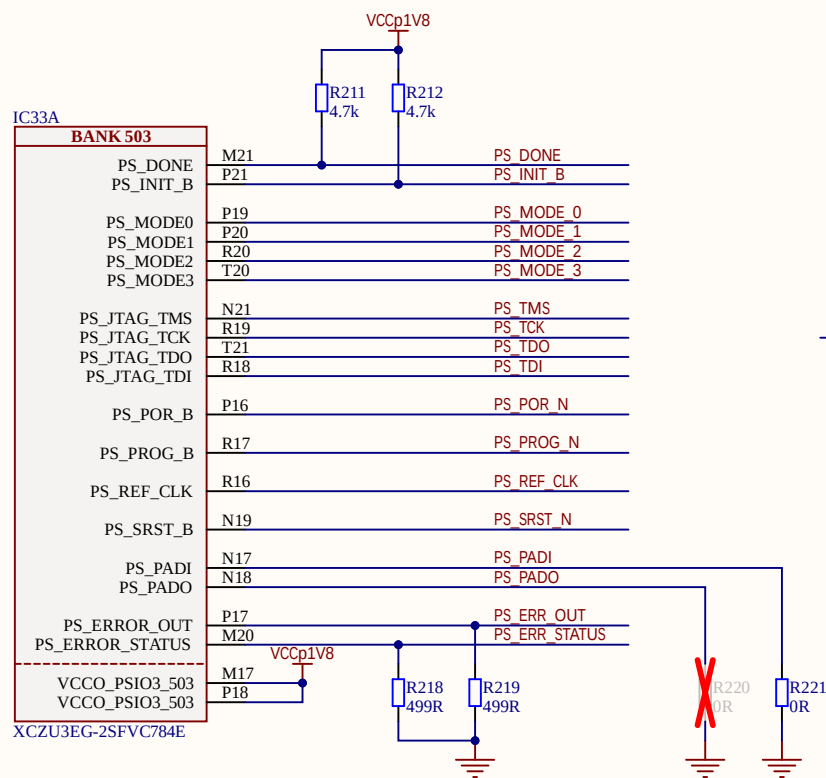
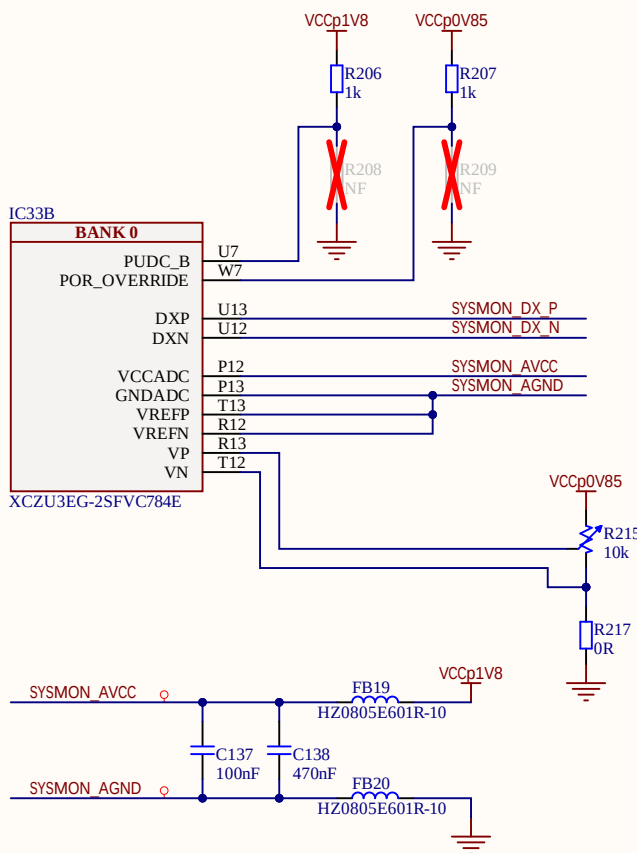
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CLOCK I:

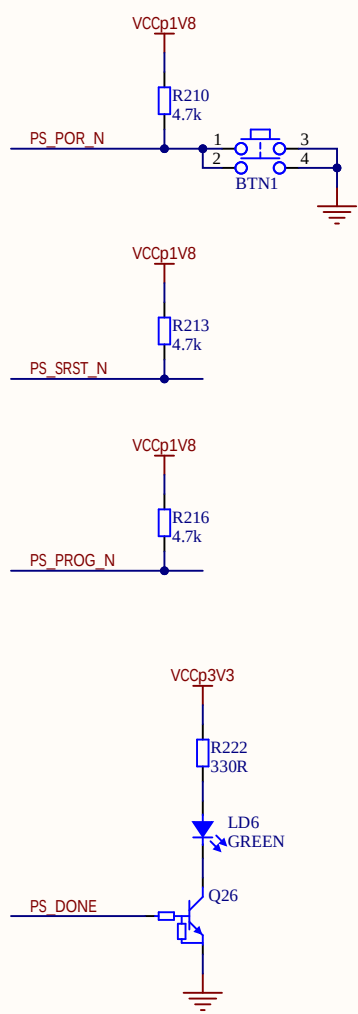


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MPSoC CONFIG

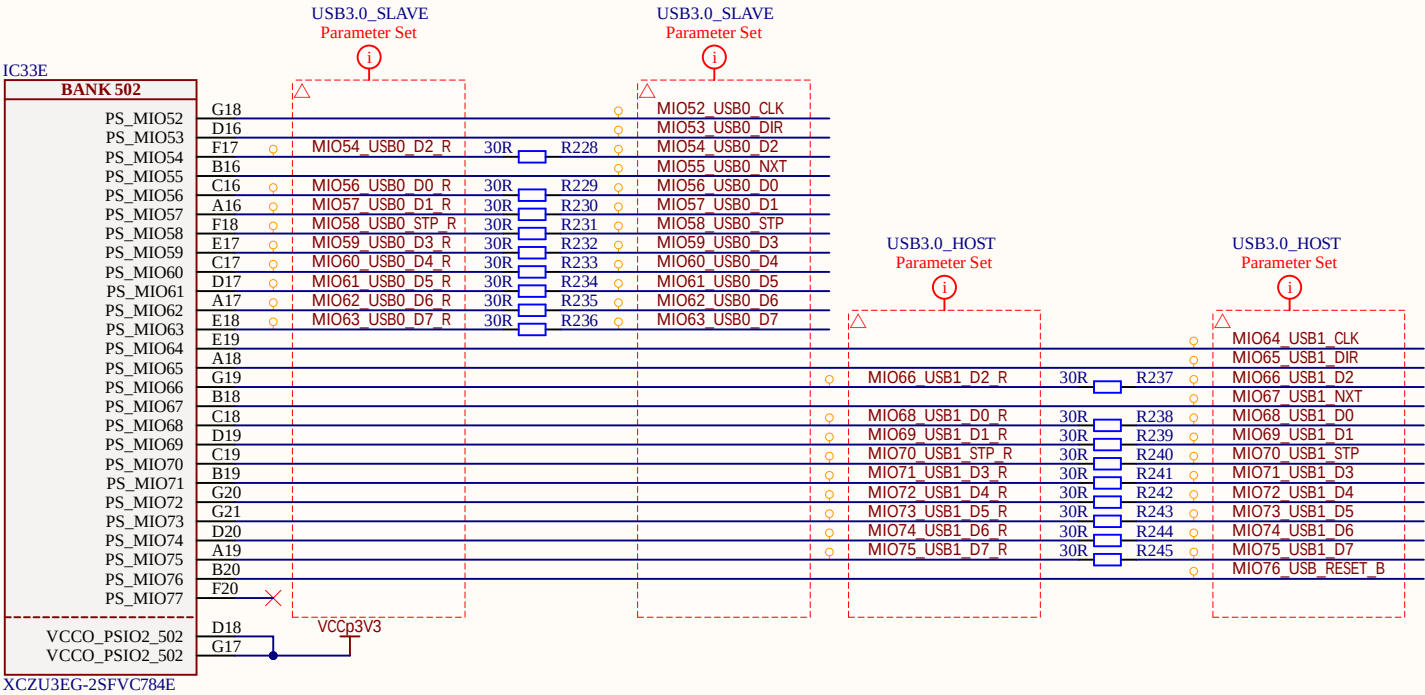
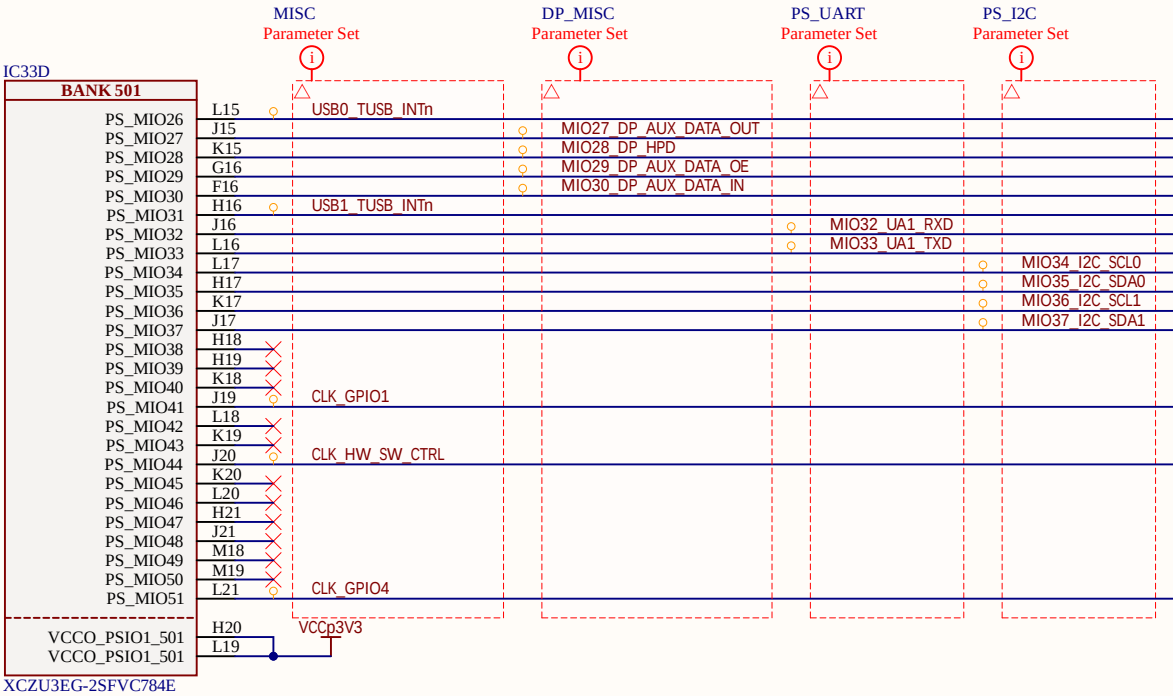
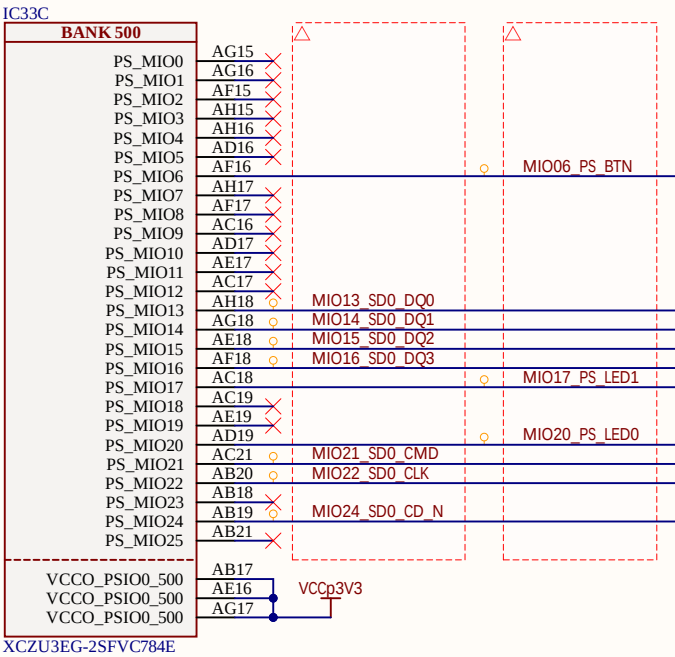


BOOT-MODE	M3	M2	M1	M0
JTAG	L	L	L	L
SD Card	L	L	H	H



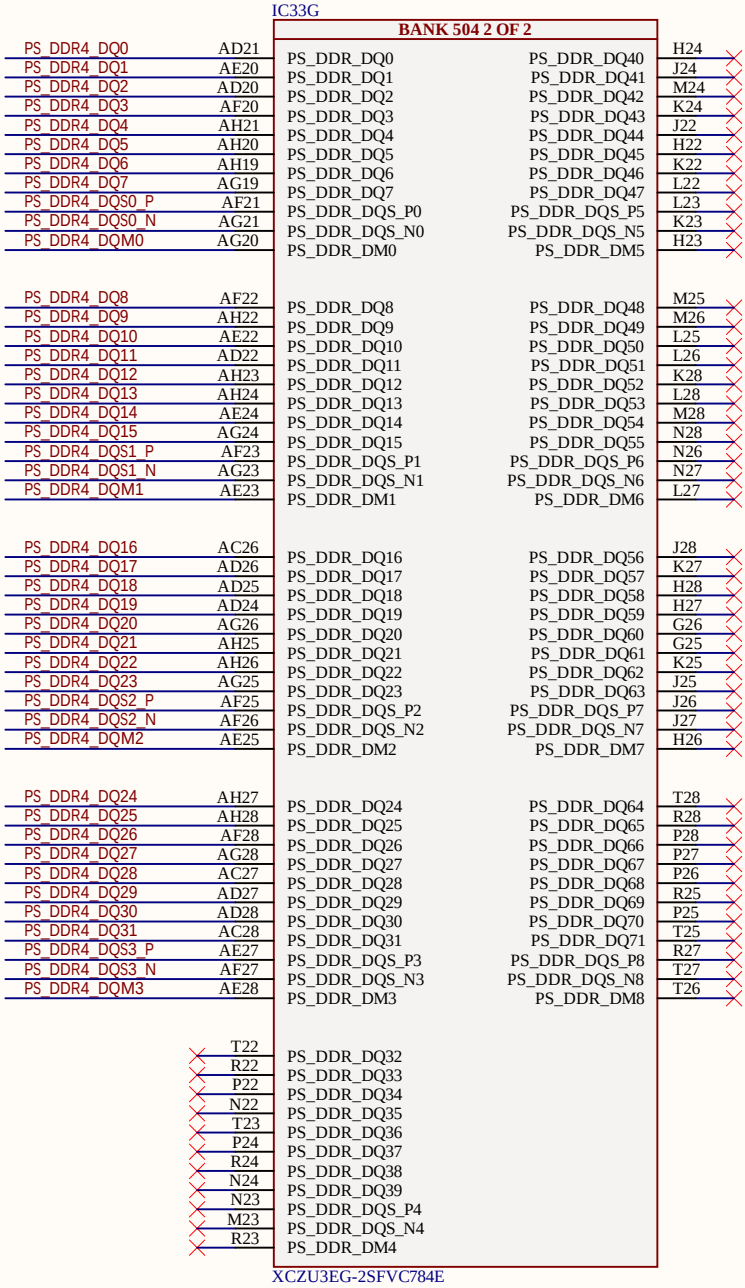
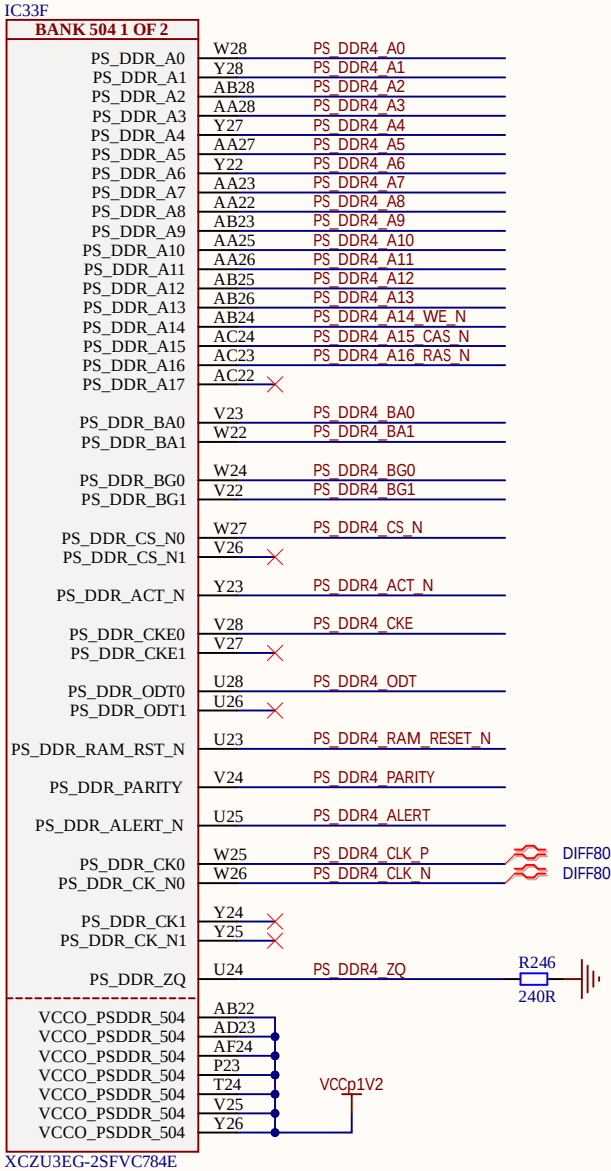
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PS: BANKS 500-502



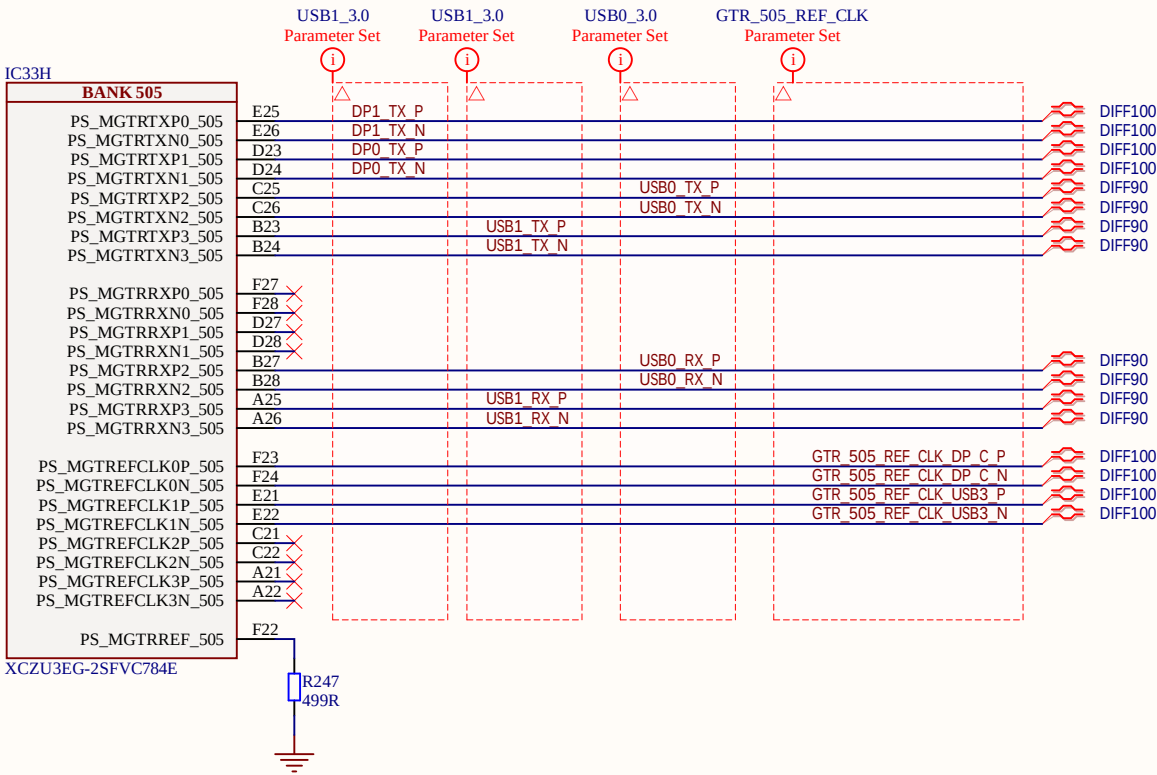
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PS: BANK 504



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PS: MGT

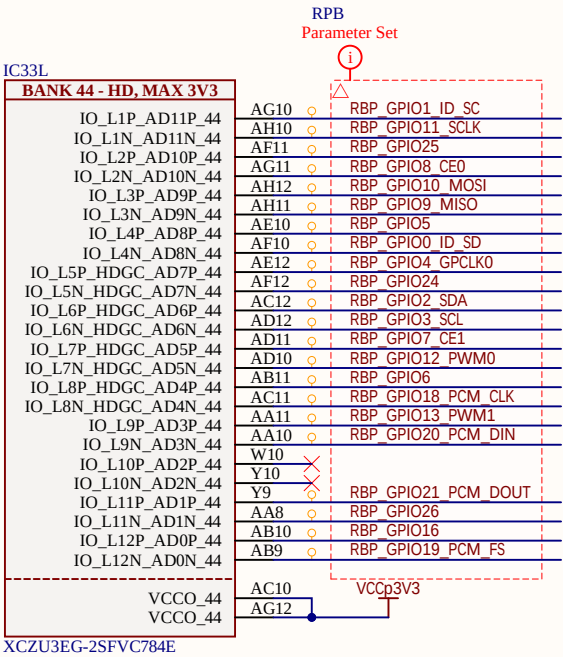
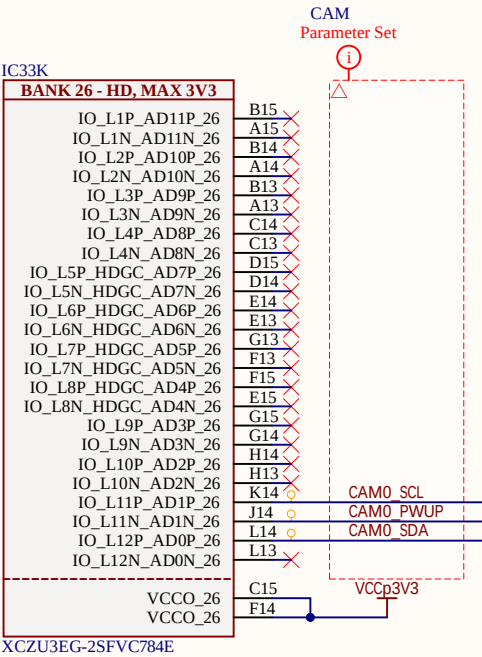
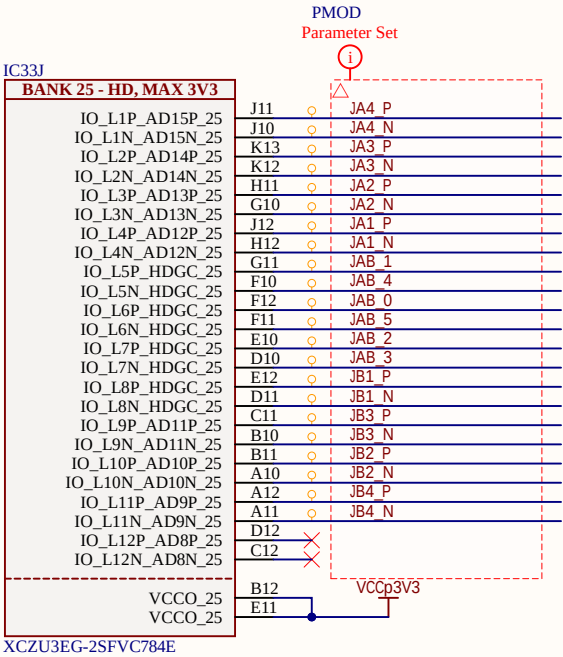
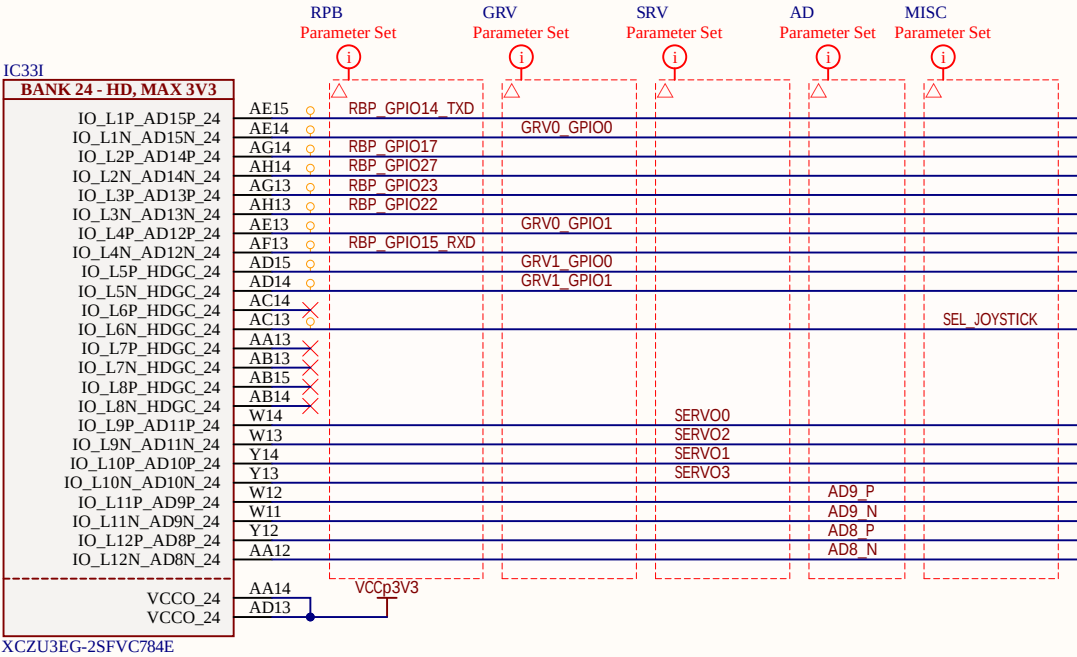


GTR_505_REF_CLK_DP_C_P	10nF	C139	GTR_505_REF_CLK_DP_P
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GTR_505_REF_CLK_USB3_C_P	10nF	C141	GTR_505_REF_CLK_USB3_P
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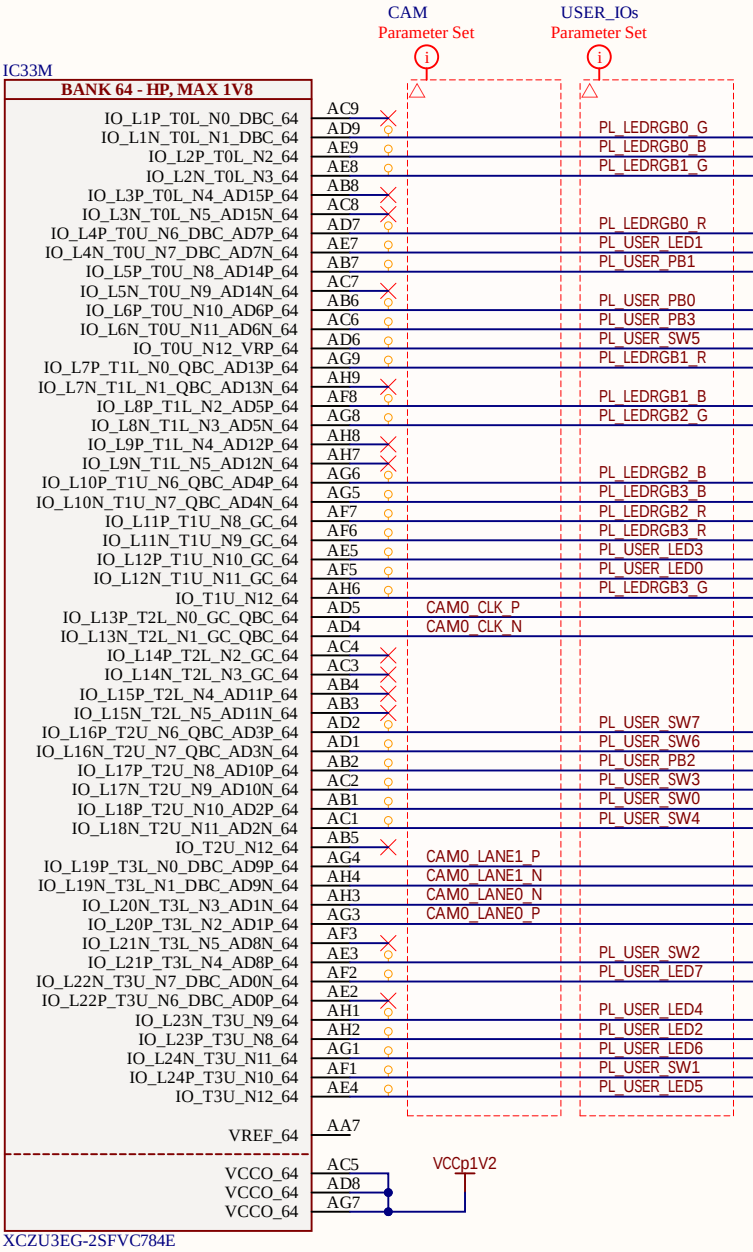
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PL: BANKS 64-66

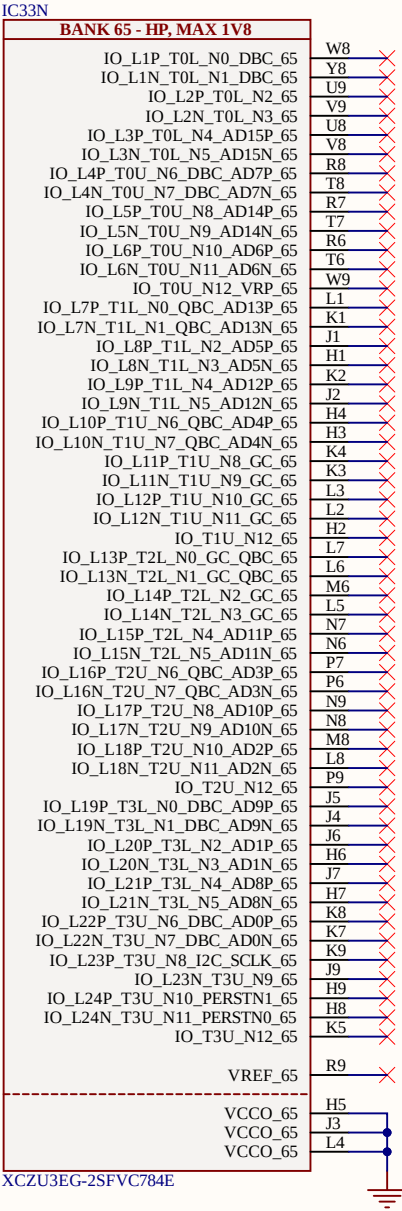


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Title: AUP-ZU3		Variant: Prototype	
Page Contents: [19] - PL BANKS 43-46.SchDoc			
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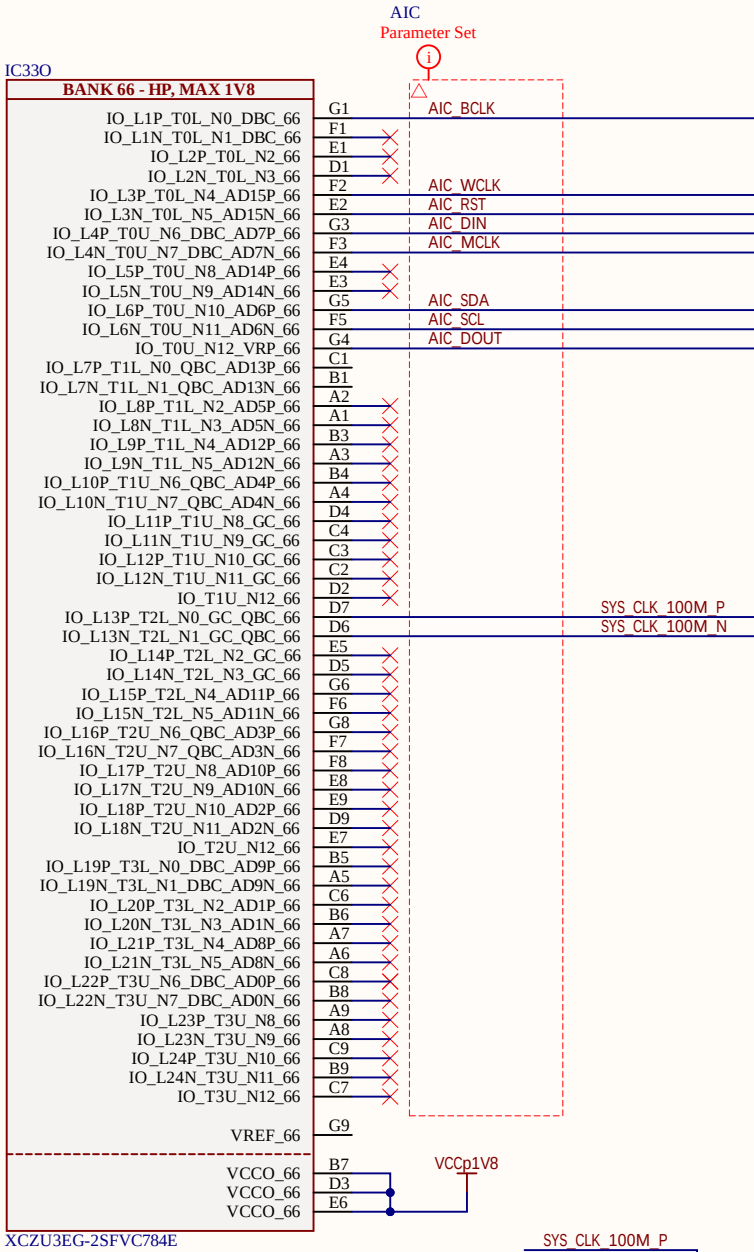
PL: BANKS 67-69



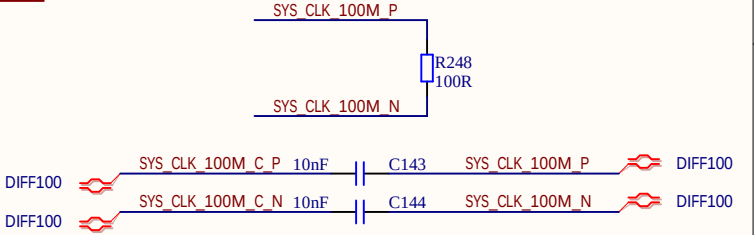
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XCZU3EG-2SFVC784E

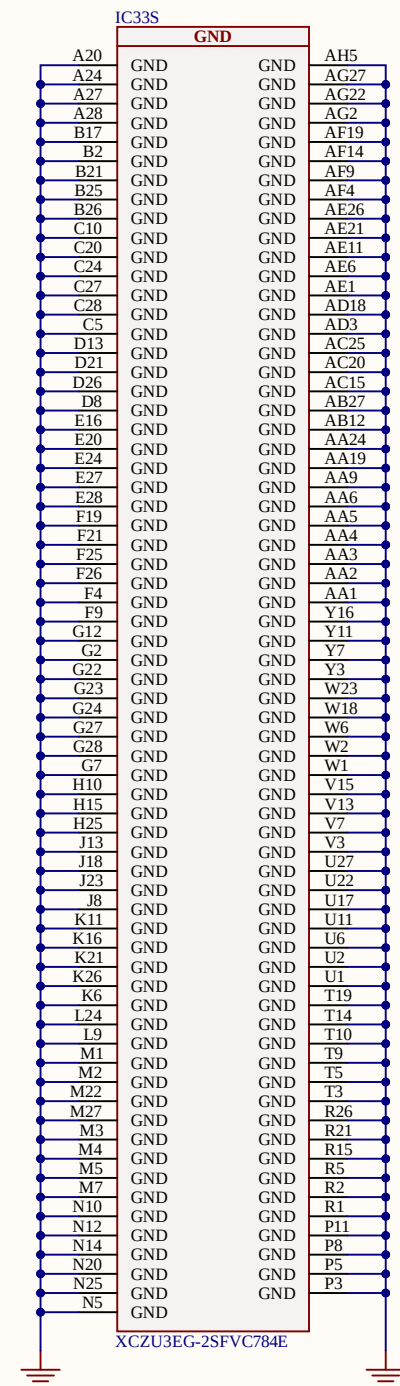
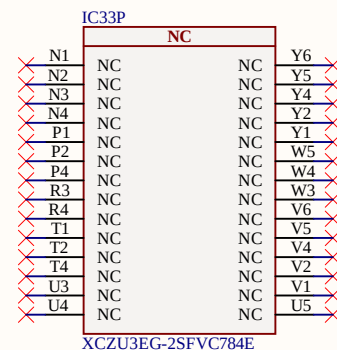
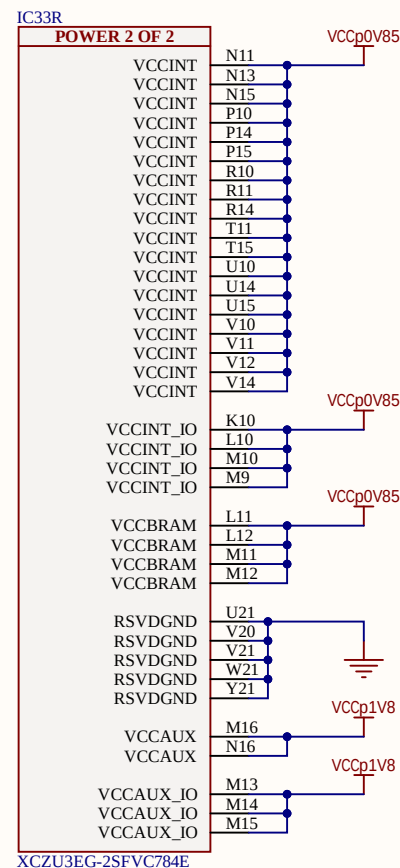
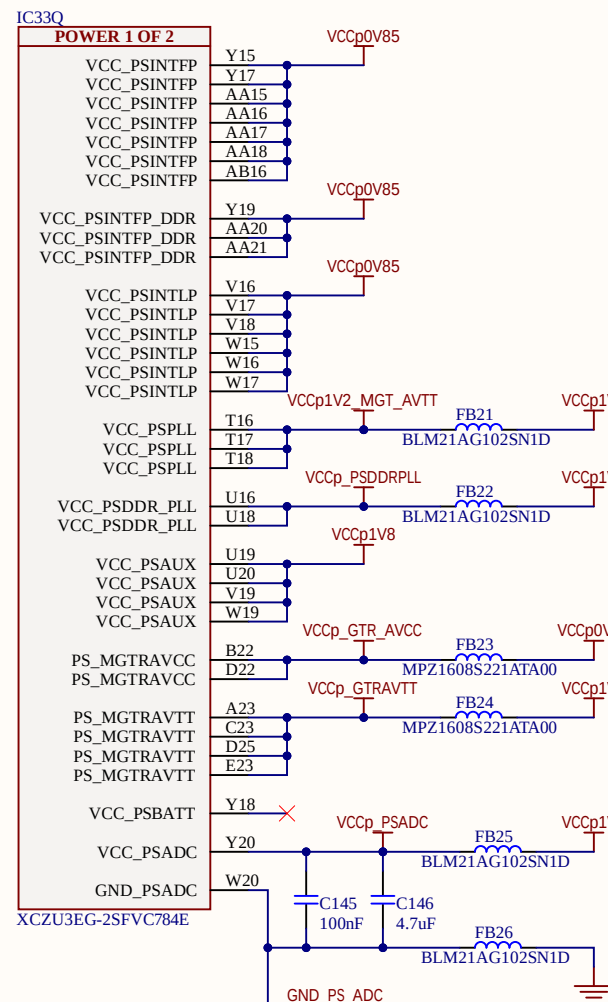


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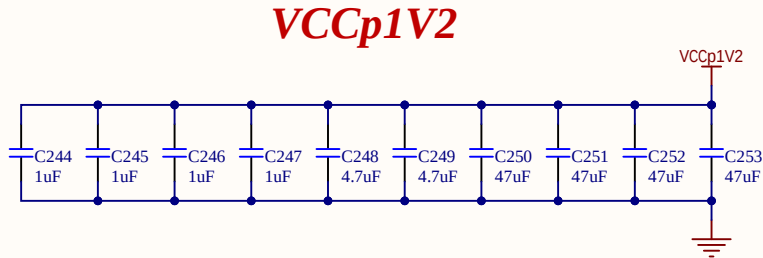
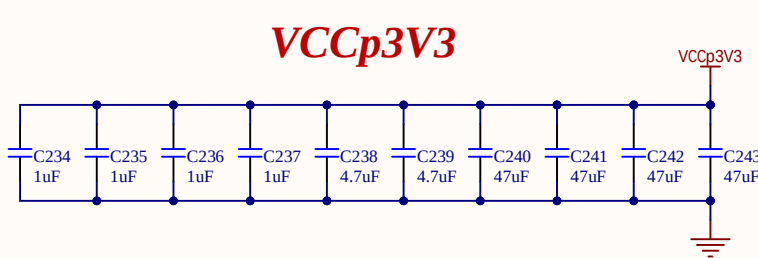
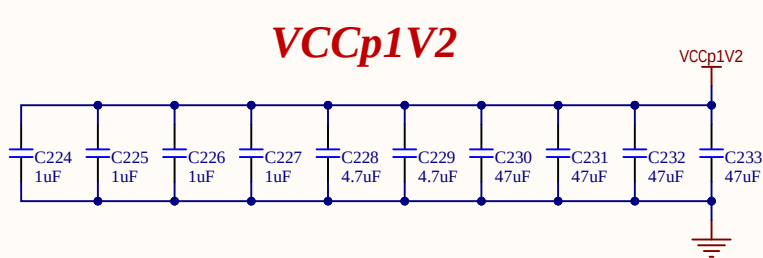
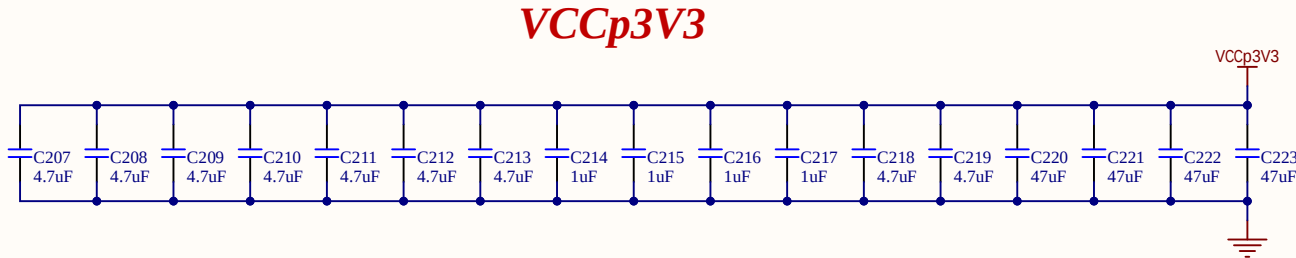
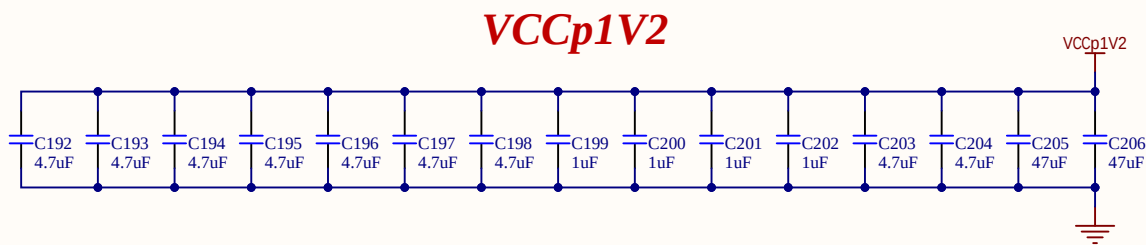
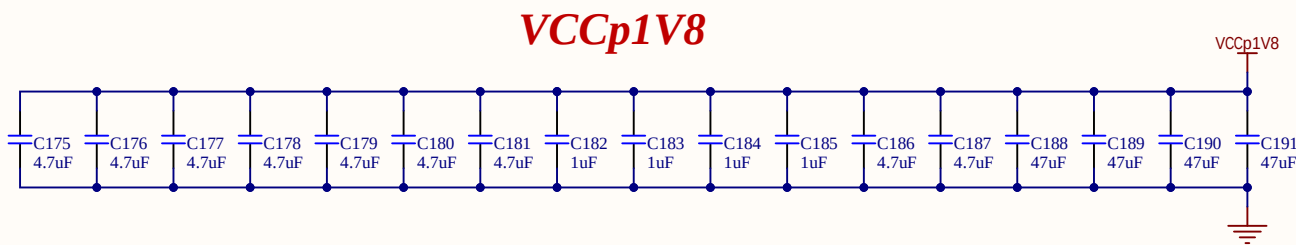
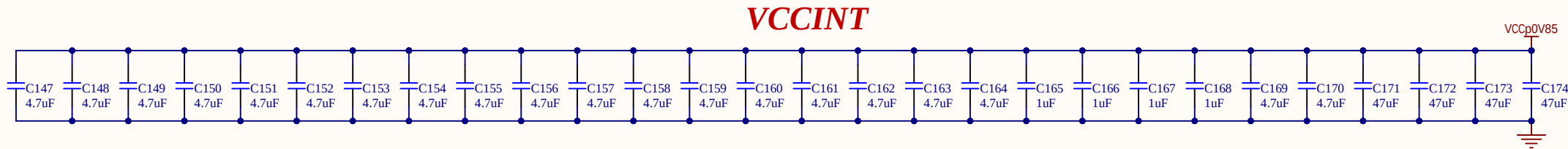
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Page Contents: [20] - PL BANKS 64-66.SchDoc			
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MPSoC PWR AND GND PINS



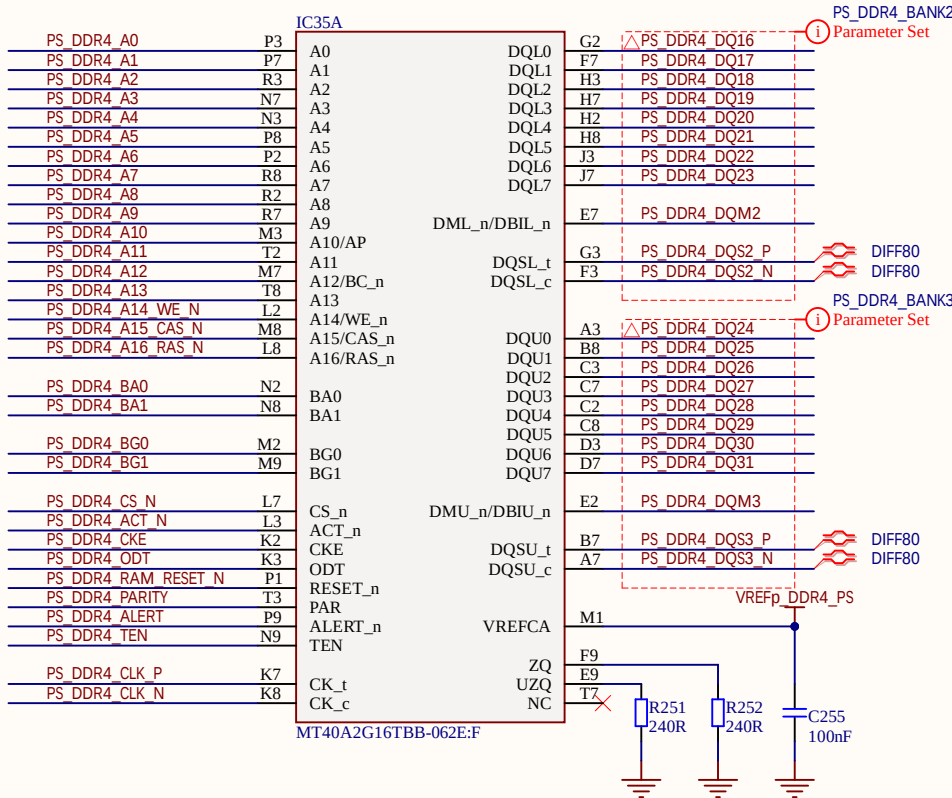
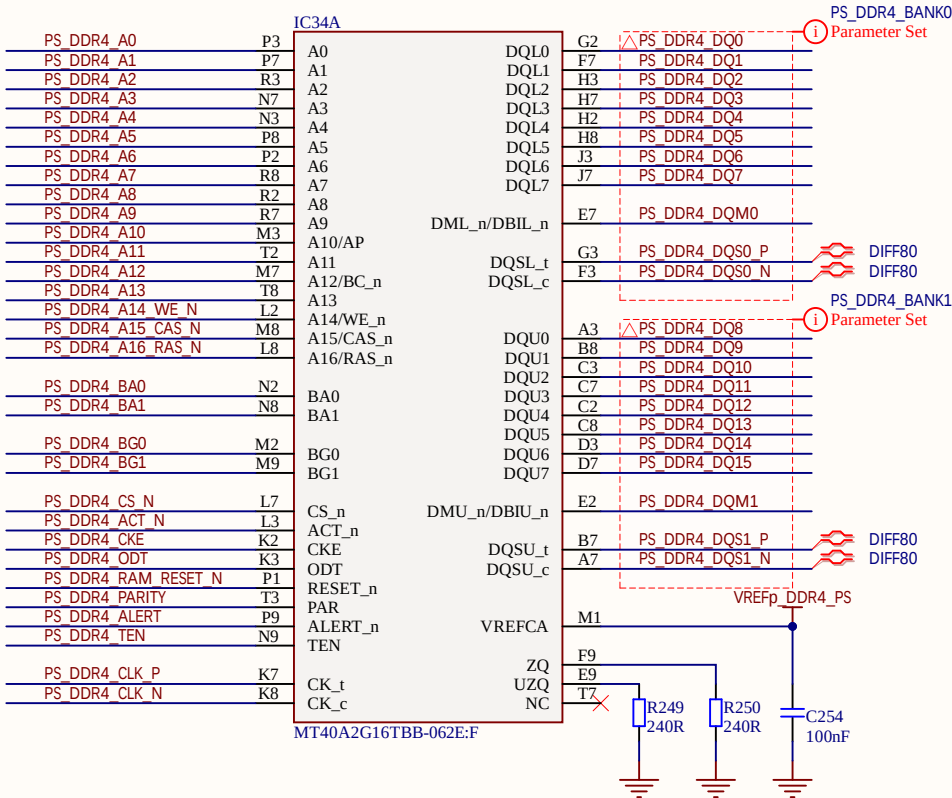
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Title: AUP-ZU3		Variant: Prototype	
Page Contents: [21] - MPSoC PWR AND GND PINS.SchDoc			
Size: A3	DWG NO: KT-2024-0015-002-001A		Revision: V3I1
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DECOUPLING



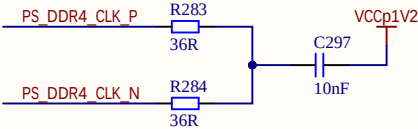
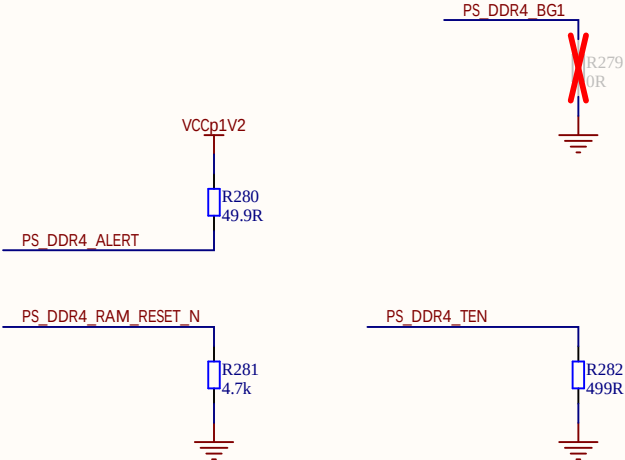
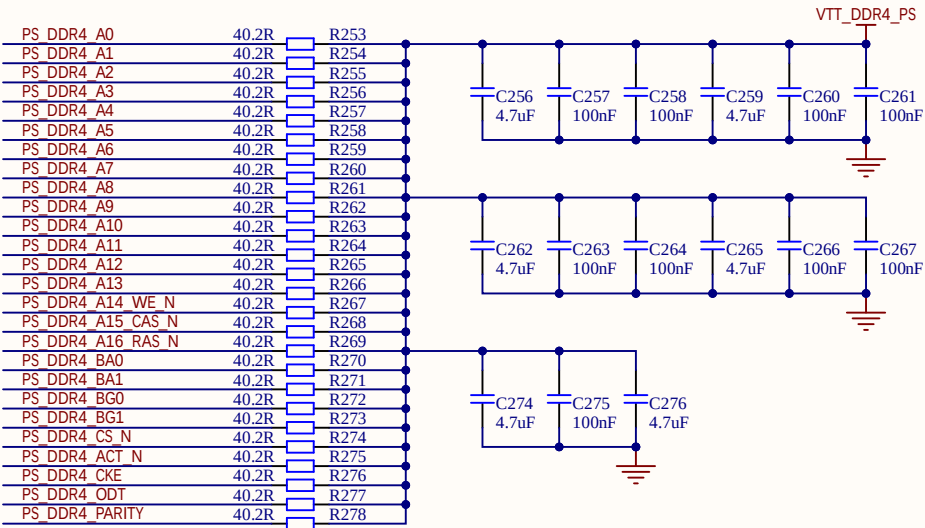
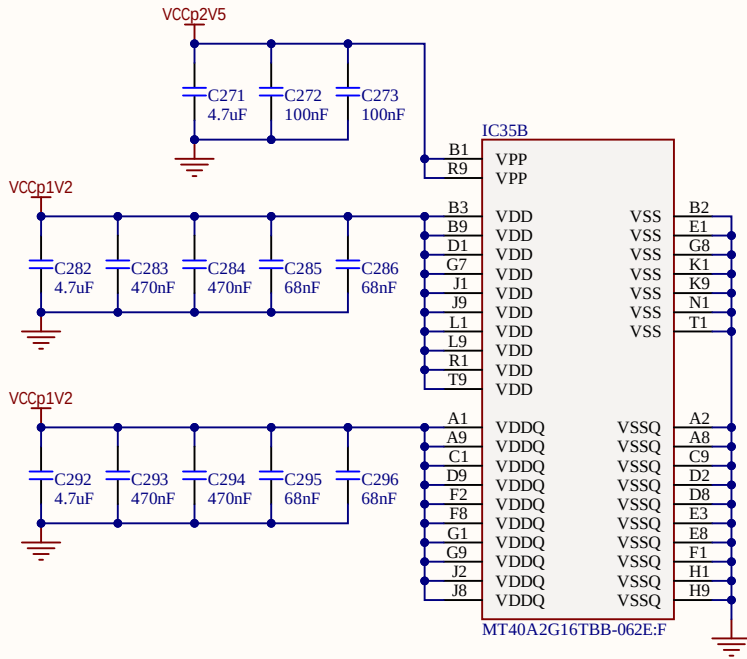
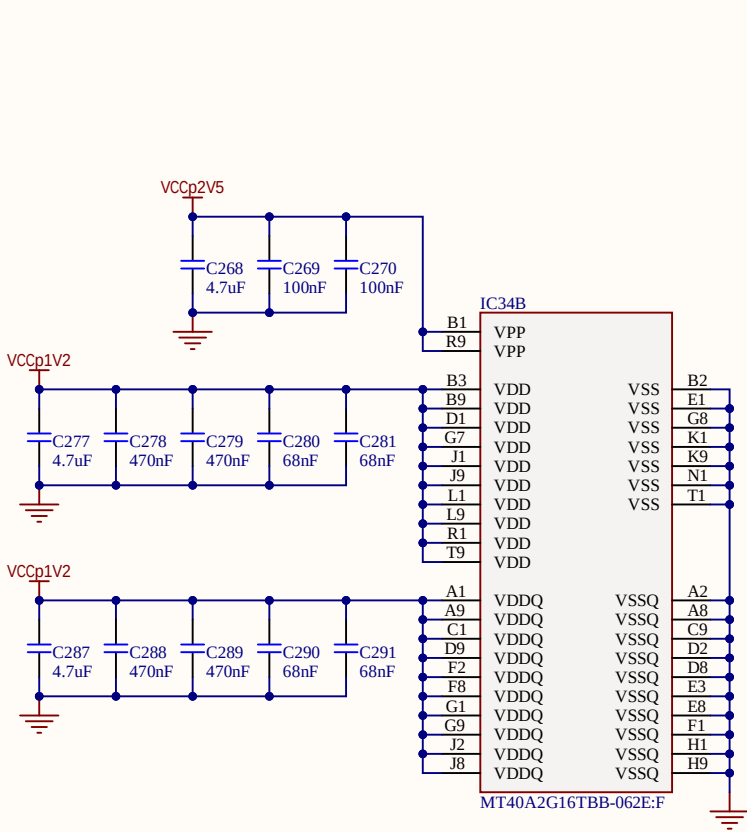
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Title: AUP-ZU3		Variant: Prototype	
Page Contents: [22] - MPSoC DECOUPLING.SchDoc			
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DDR4 MEMORY PS I



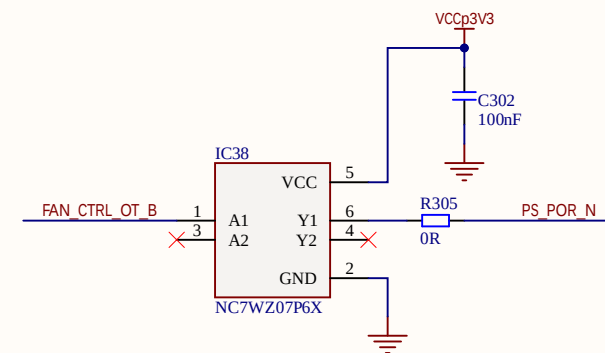
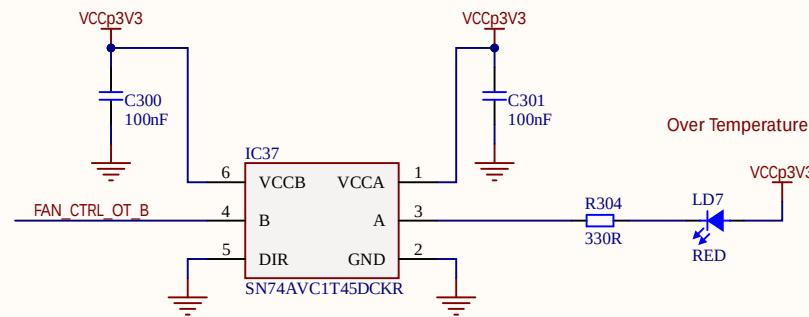
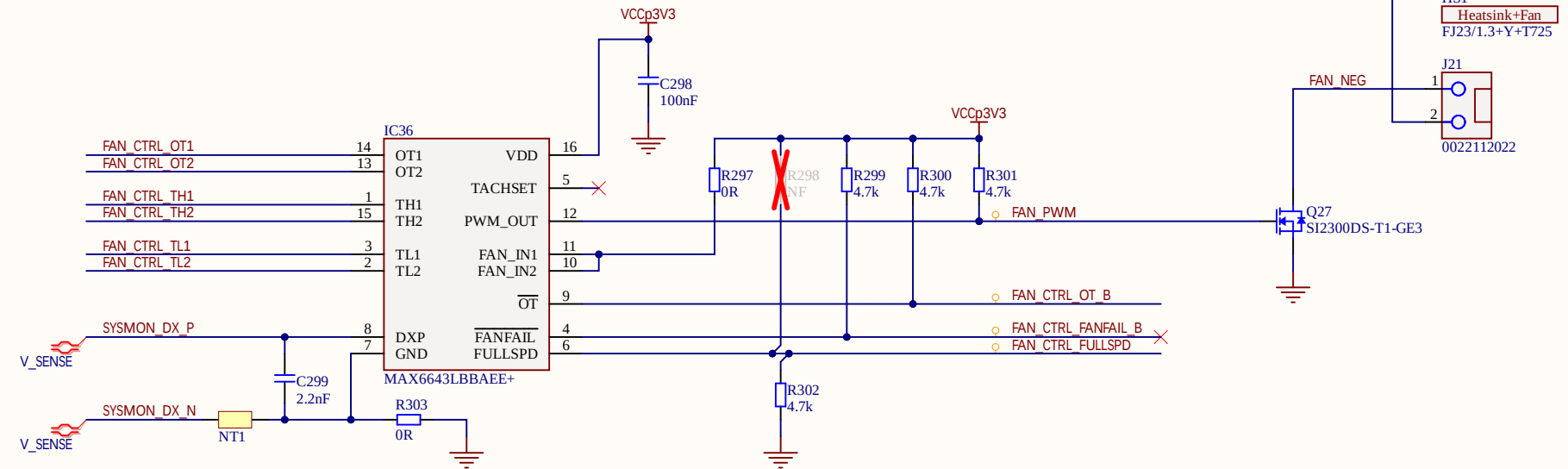
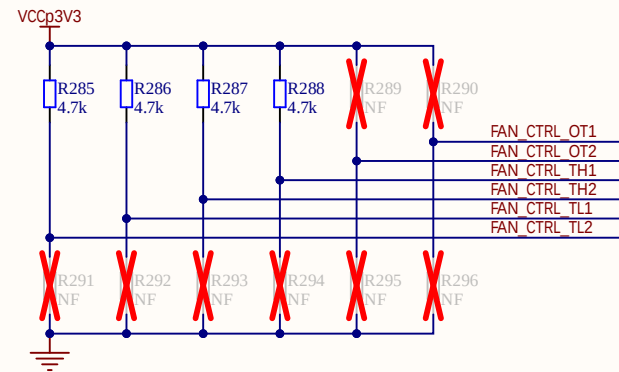
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Title: AUP-ZU3		Variant: Prototype	
Page Contents: [23] - DDR4 MEMORY PS I.SchDoc			
Size: A3	DWG NO: KT-2024-0015-002-001A		Revision: V3I1
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DDR4 MEMORY PS II



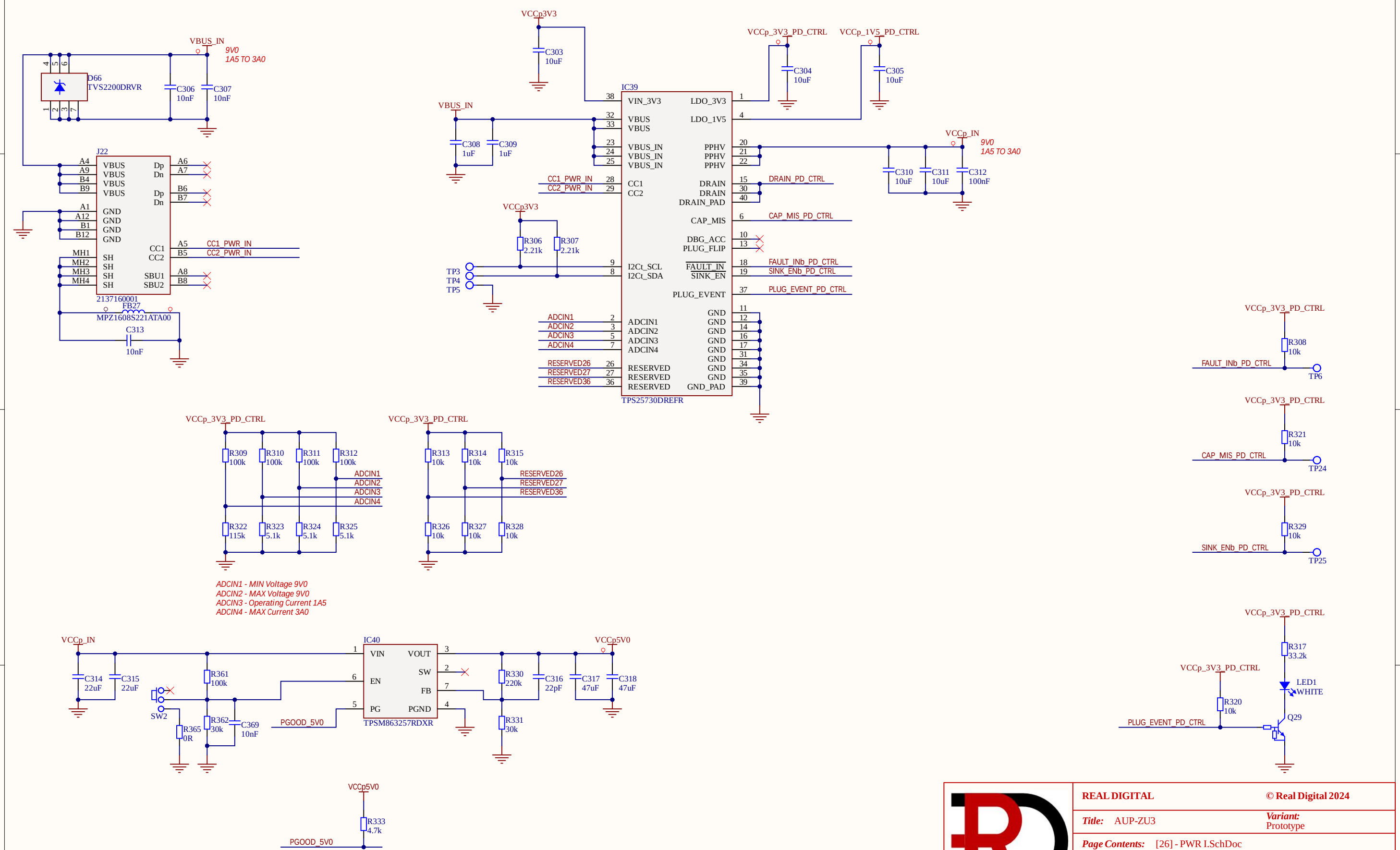
REAL DIGITAL		© Real Digital 2024	
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Page Contents: [24] - DDR4 MEMORY PS II.SchDoc			
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FAN CONTROLLER



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POWER I

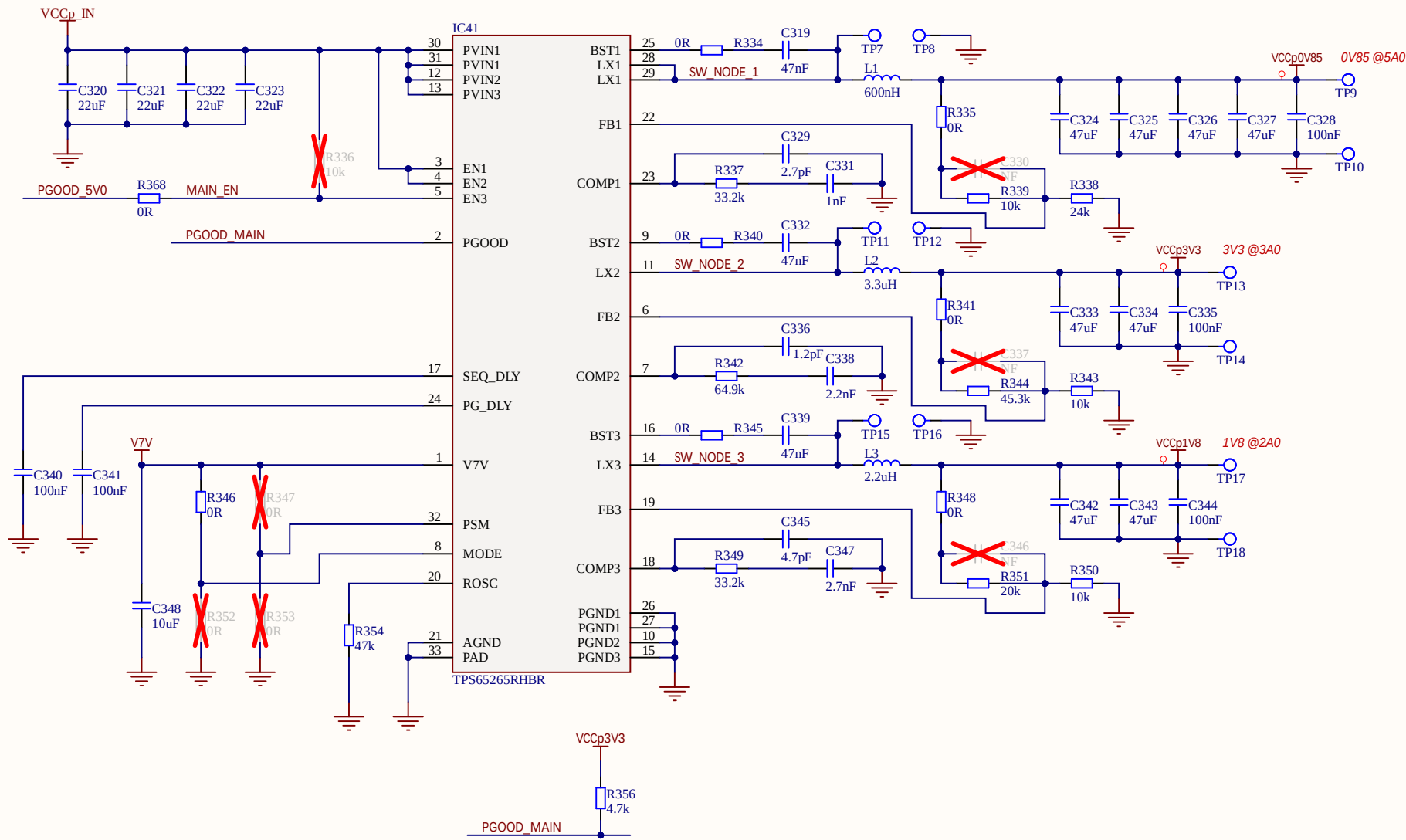


ADCIN1 - MIN Voltage 9V0
ADCIN2 - MAX Voltage 9V0
ADCIN3 - Operating Current 1A5
ADCIN4 - MAX Current 3A0



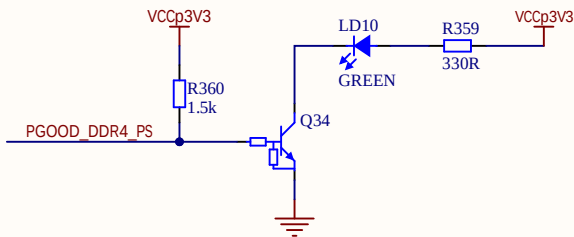
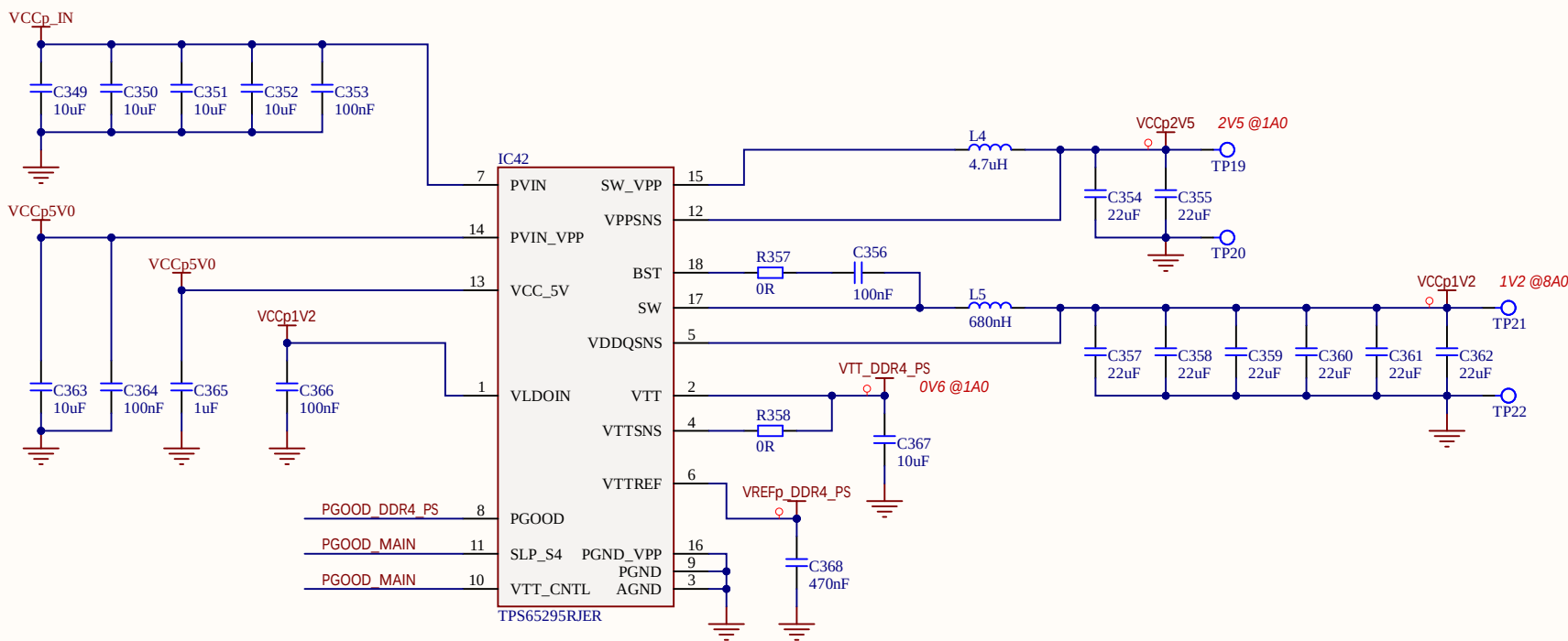
REAL DIGITAL		© Real Digital 2024	
Title: AUP-ZU3		Variant: Prototype	
Page Contents: [26] - PWR I.SchDoc			
Size: A3	DWG NO: KT-2024-0015-002-001A		Revision: V3I1
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POWER II



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POWER III

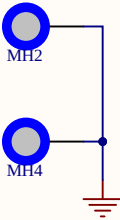
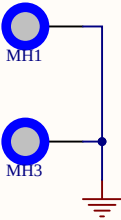


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Title: AUP-ZU3		Variant: Prototype	
Page Contents: [28] - PWR III.SchDoc			
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MECHANICAL AND POWER SEQUENCING

Real Digital
LG1

AMD-AUP
LG2



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Title: AUP-ZU3		Variant: Prototype	
Page Contents: [29] - MECH AND PWR SEQUENCING.SchDoc			
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DOC: REVISION HISTORY

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	Size: A3	DWG NO: KT-2024-0015-002-001A		Revision: V3I1
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